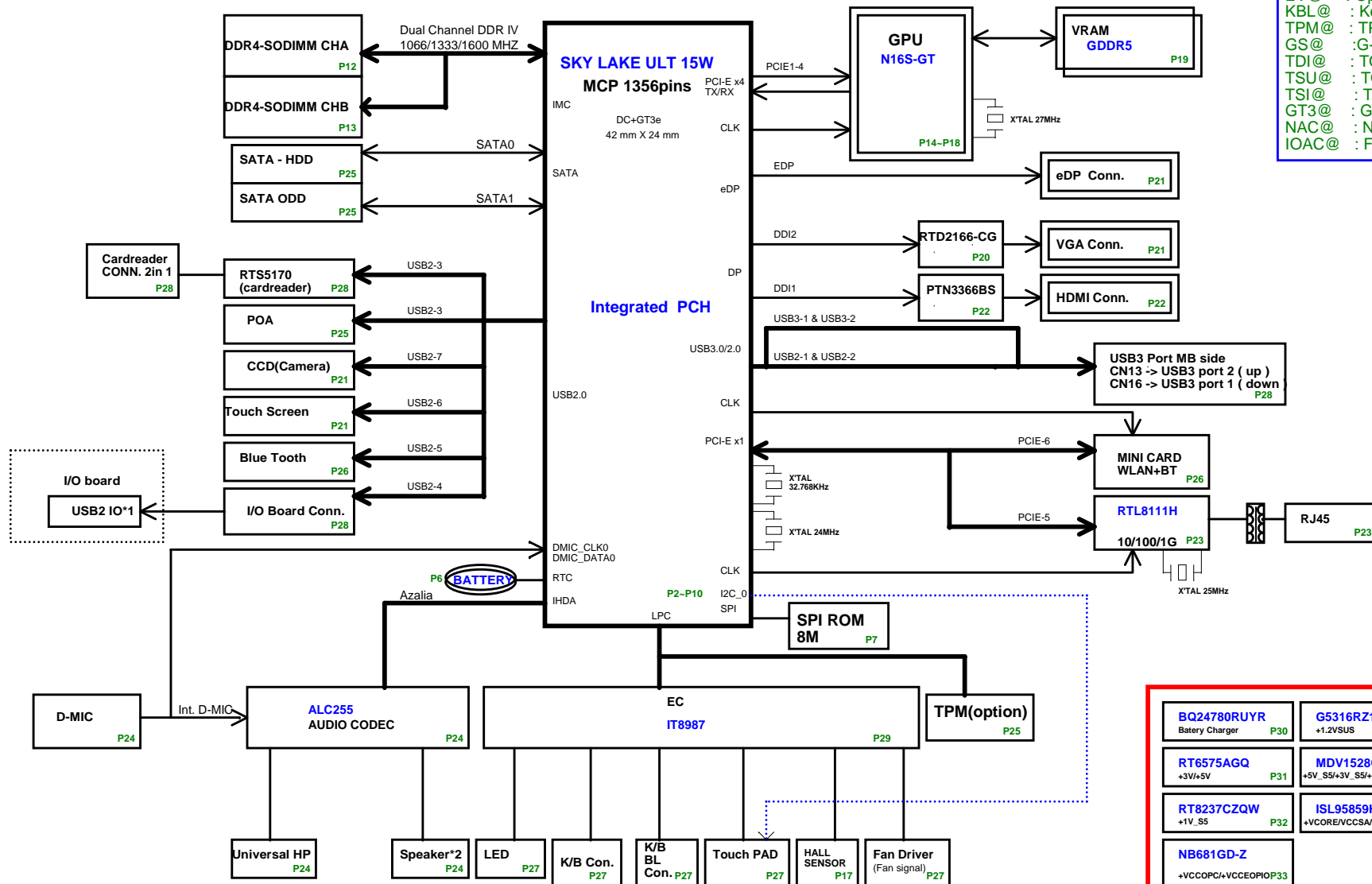


# Z8V Serials SKL ULT SYSTEM BLOCK DIAGRAM



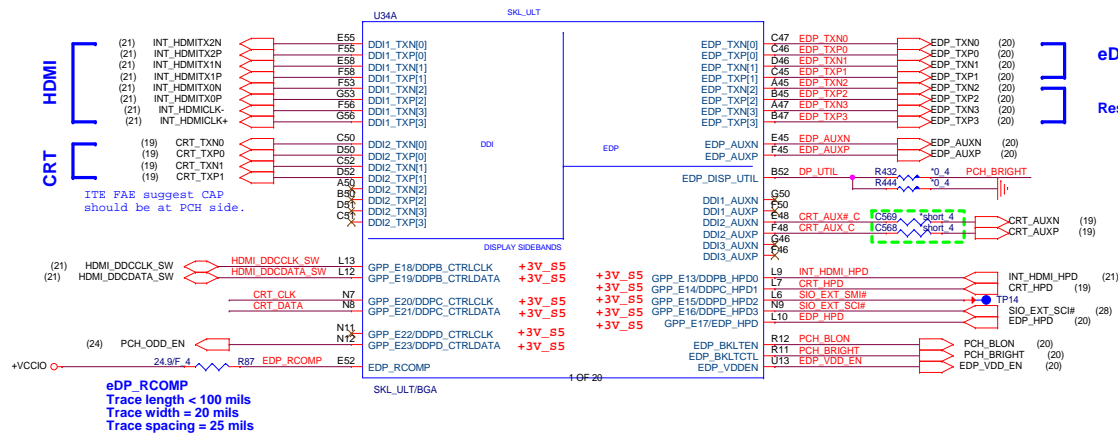
## BOM

IV@	: iGPU
EV@	: Optimus
KBL@	: Keyboard backlight
TPM@	: TPM
GS@	: G-SENSOR
TDI@	: TOUCH PAD I2C
TSU@	: TOUCH SCREEN USB
TSI@	: TOUCH SCREEN I2C
GT3@	: GT3 CPU
NAC@	: Non IOAC
IOAC@	: For IOAC

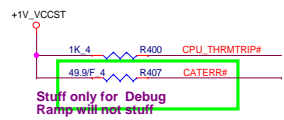
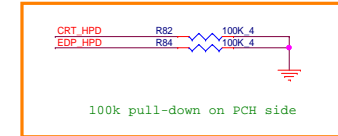
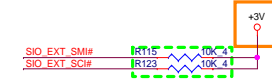
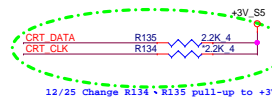
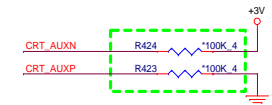
<b>BQ24780RUYR</b> Battery Charger P30	<b>G5316RZ1D</b> +1.2VSUS P34	<b>Thermal Protection</b> Discharger P38
<b>RT6575AGQ</b> +3V/+5V P31	<b>MDV1528Q</b> +5V_SS/+3V_SS/+3V/+5V P31	<b>UP1658RQKF</b> +VGPU CORE P39
<b>RT8237CZQW</b> +1V_SS P32	<b>ISL95859HRTZ-T</b> +VCORE/VCCSA/VCCGT P35	<b>RT8068AZQW</b> +1.05V_GFX/+3V_GFX +1.5V_GFX P40
<b>NB681GD-Z</b> +VCCOPC/+VCCOPROP33		



## Skylake ULT (DISPLAY,eDP)



Don't stuff if we use DP to VGA IC



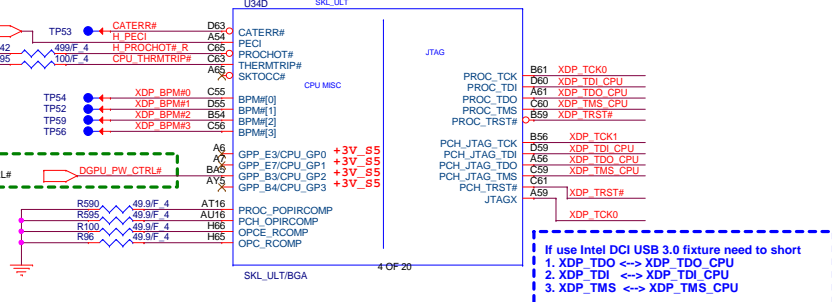
**H\_PECI (50ohm)**  
Route on microstrip only  
Spacing >18 mils  
Trace Length: 0.4~6.125 inches



**BPM#[0:7]**  
Trace Length 1~6 inches  
Length match < 300 mils

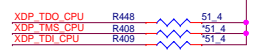


**SM\_RCOMP[0:2]**  
Trace length < 500 mils  
Trace width = 12~15 mils  
Trace spacing = 20 mils



**PCH JTAG**  
JTAG\_TCK,JTAG\_TMS  
Trace Length < 9000mils

**TCK,TMS**  
Trace Length < 9000mils

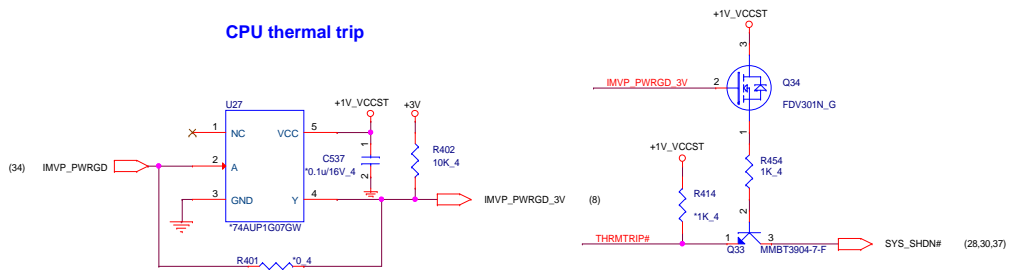


**H\_PWRGOOD (50ohm)**  
Trace Length: 1~11.25 inches



XDP\_TCK1,XDP\_TMS  
don't need pull up or pull down  
XDP\_TCK0 R558 Stuff

## CPU thermal trip



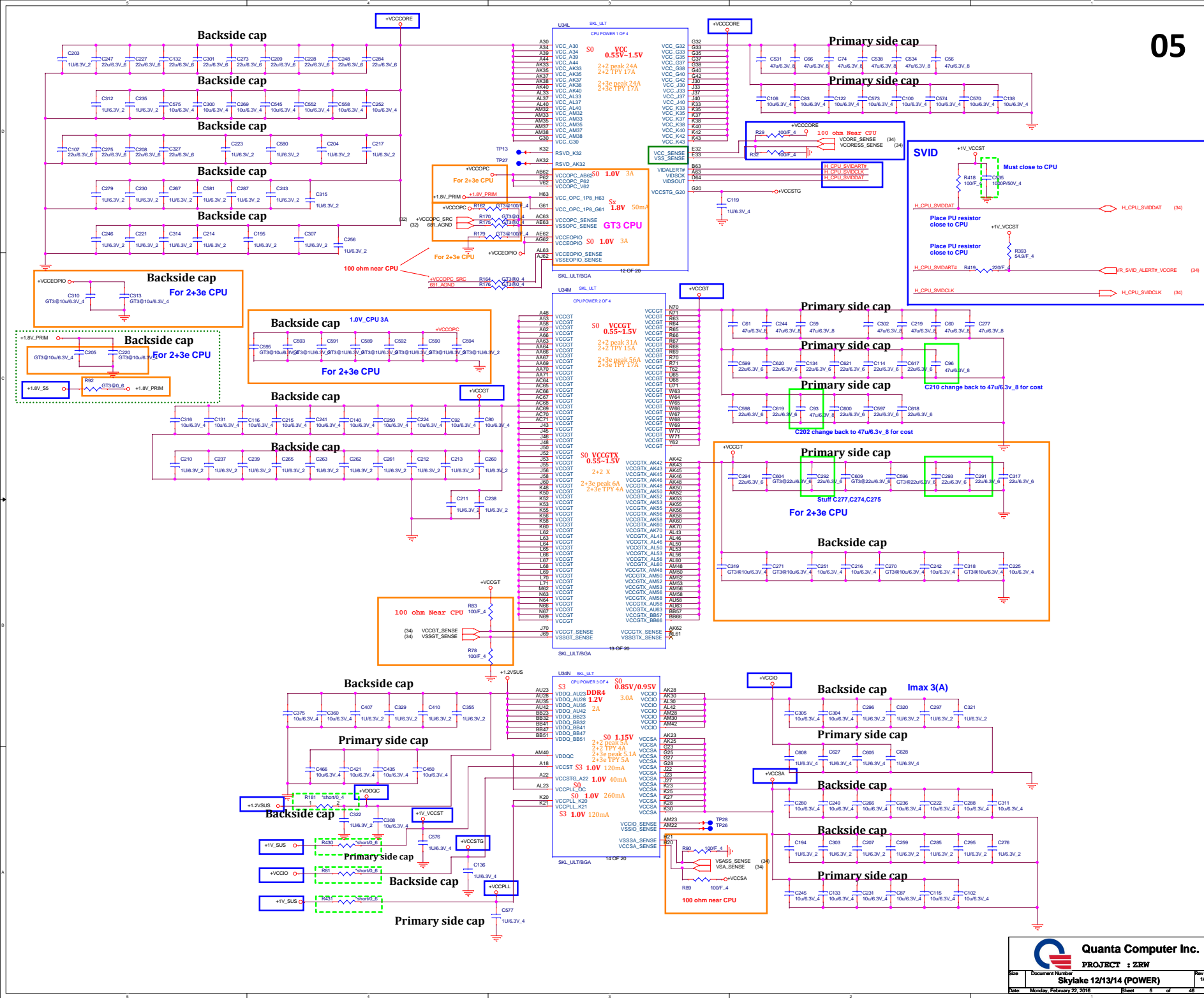




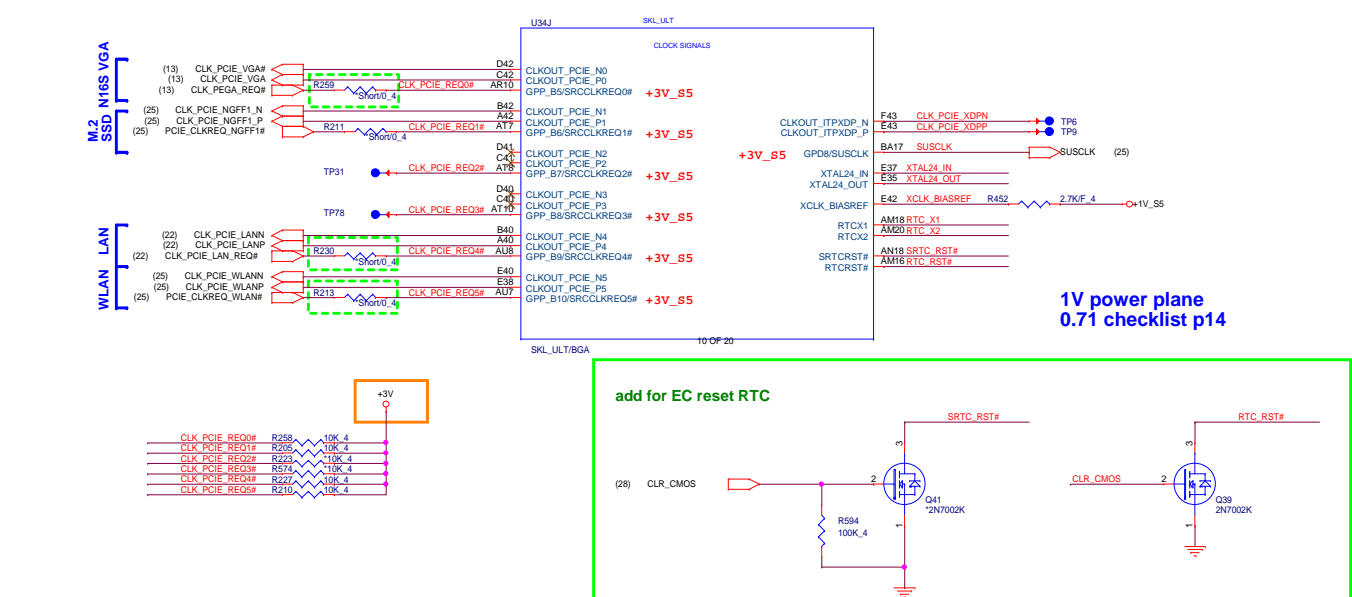
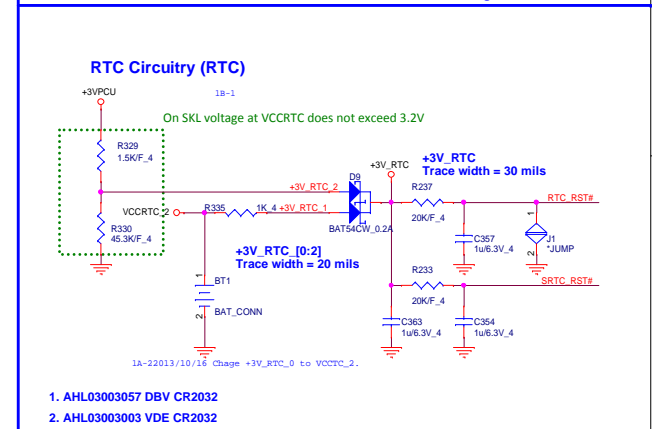
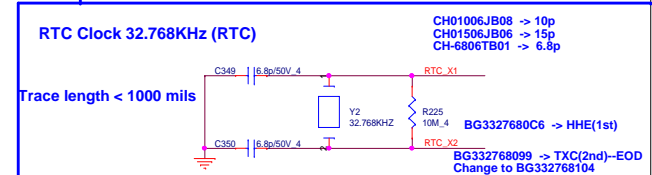
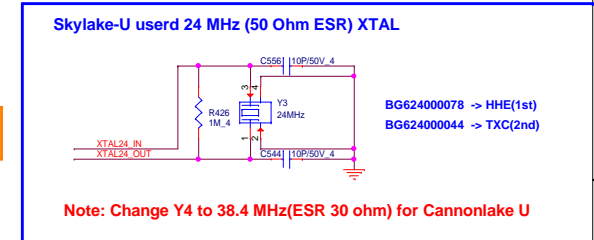
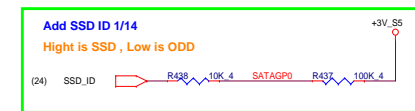
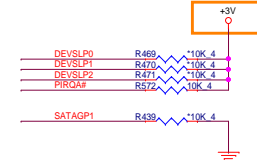
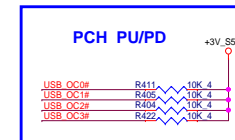




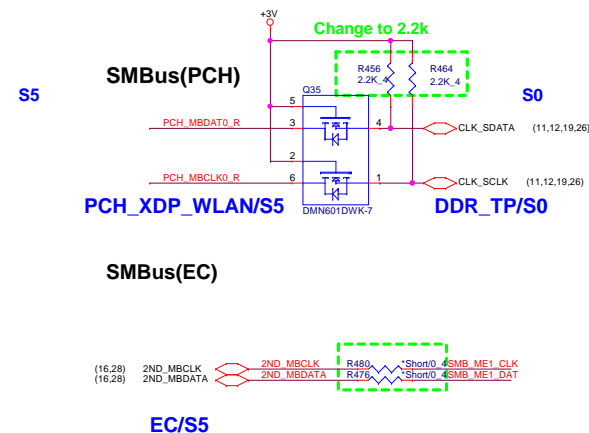






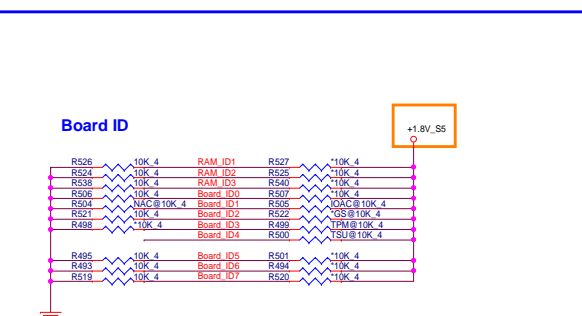
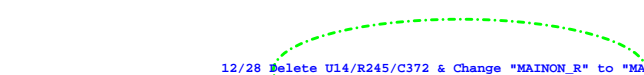
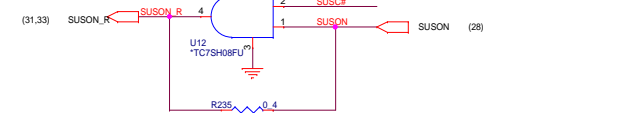
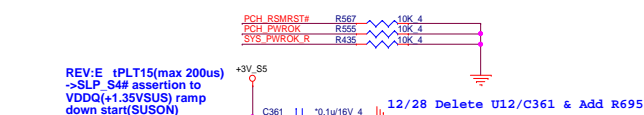
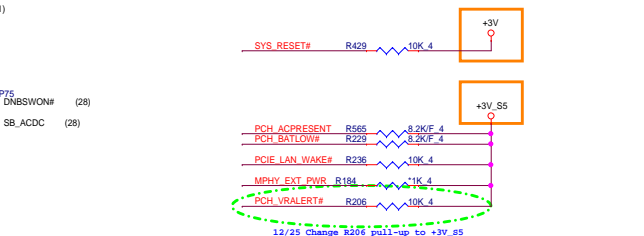
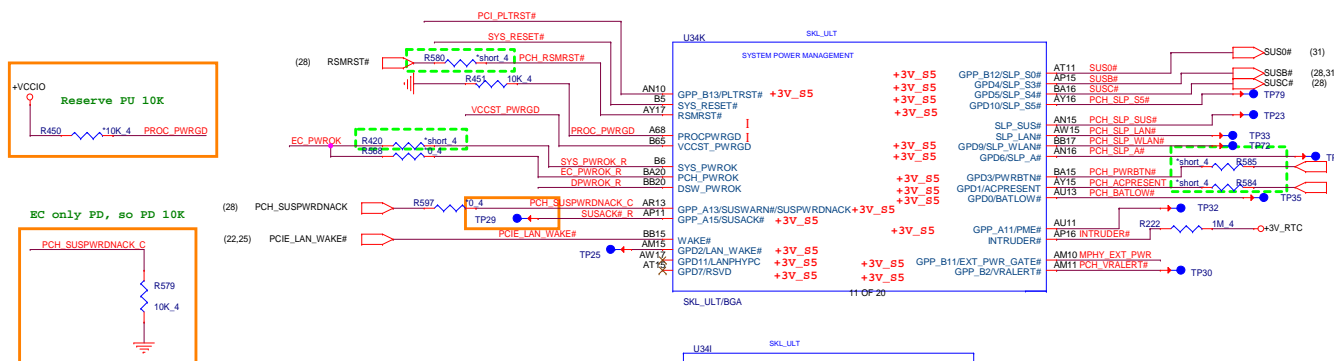




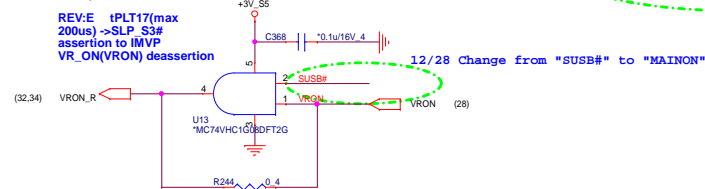
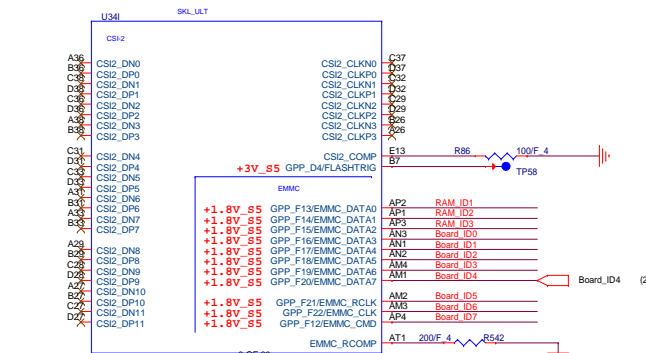


SPI ROM	Vender	Size	Quanta P/N	Vender P/N
Skylake 3.3V	WND	8M	AKE3EFP0N07	W25Q64FVSSIQ
	GGD	8M	AKE2EZN0Q00	GD25B64CSIGR

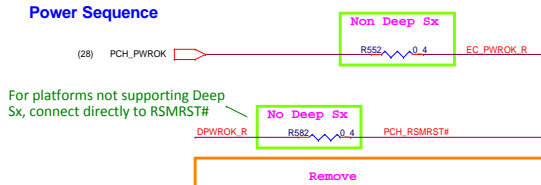




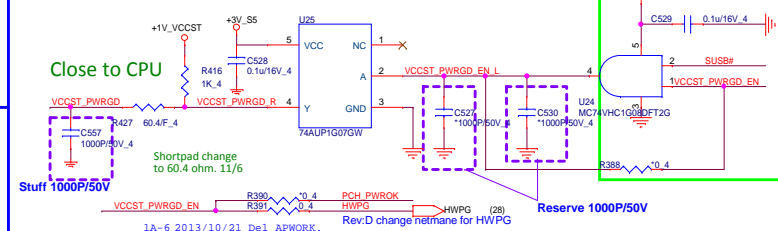
	Low	High		Low	High
BOARD_ID0	VRAM X32 (R506)	VRAM X16 (R507)	BOARD_ID5	For 14" (R495)	For 15" / 17" (R501)
BOARD_ID1	Non IOAC (R504)	IOAC (R505)	BOARD_ID6	Reserved (Default)	Reserve
BOARD_ID2	Non G-sensor (R521)	G-sensor (R522)	BOARD_ID7	Reserved (Default)	Reserve
BOARD_ID3	No TPM (R498)	TPM (R499)			
BOARD_ID4	No-Touch panel	Touch panel (R500)			



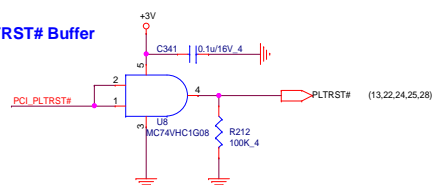
## Power Sequence



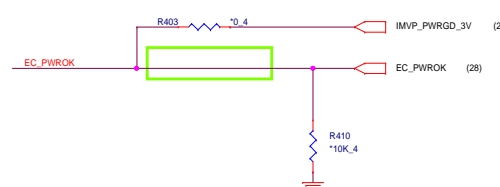
VCCST PWRGD CRB is via +1.05V PG



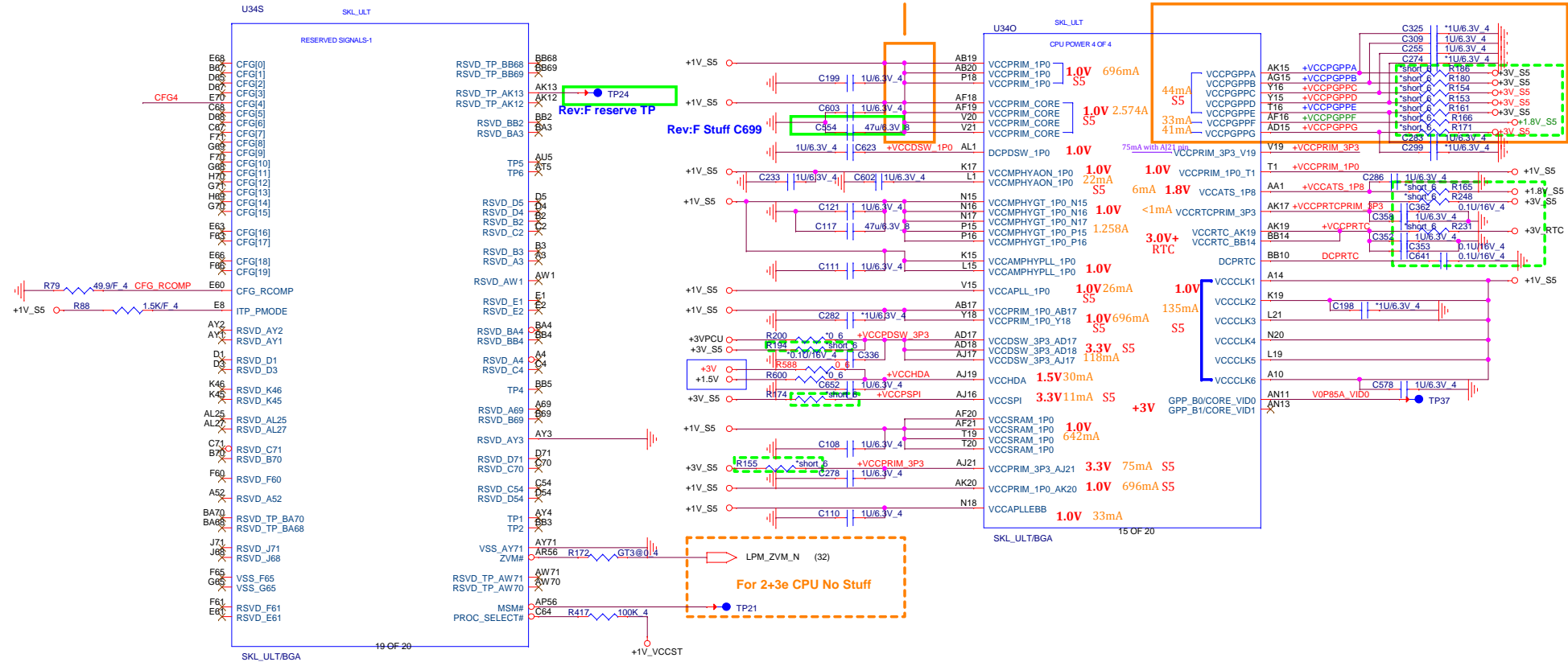
### PLTRST# Buffer




## SYSPWOK



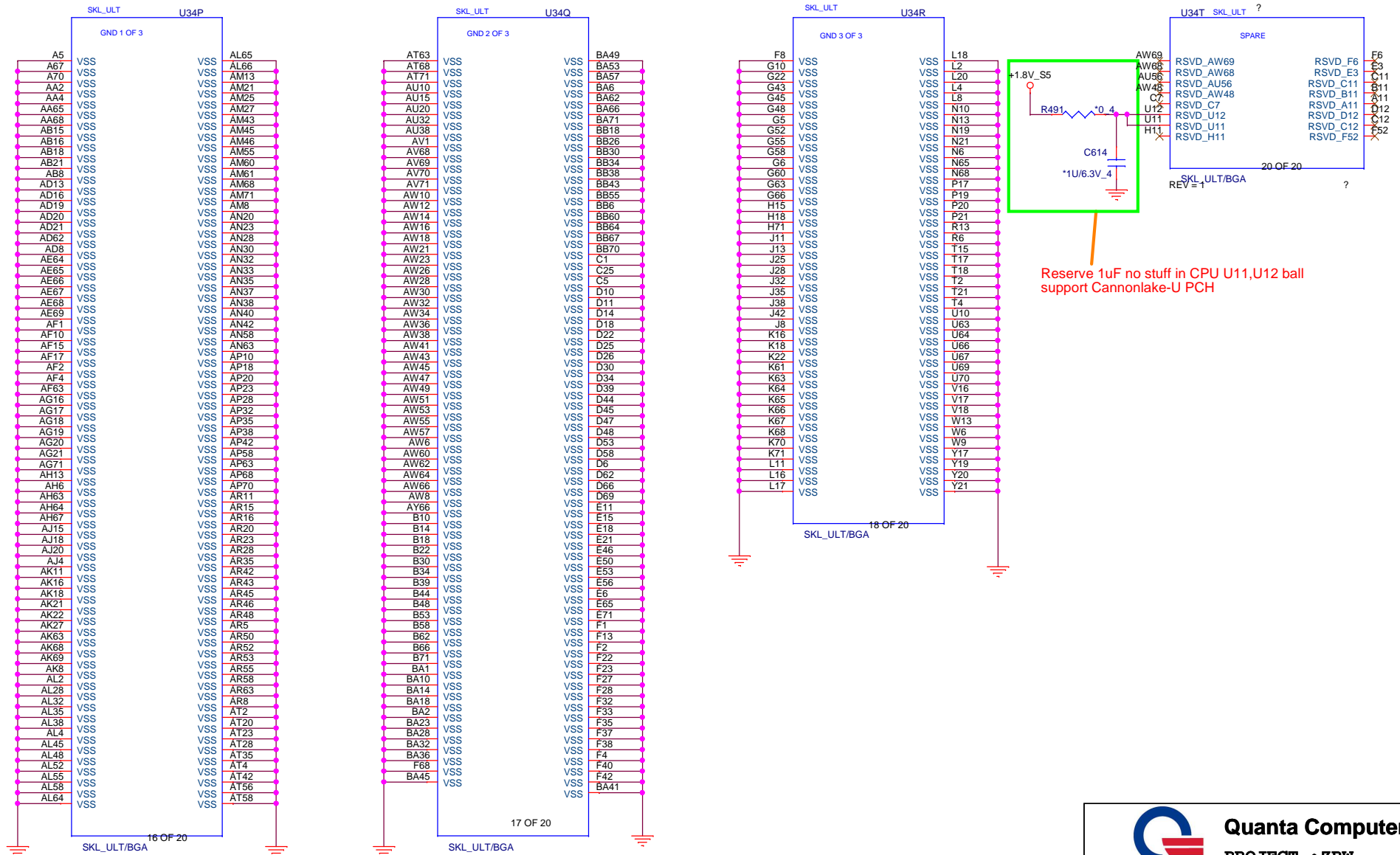




Pin Name	Strap description	Configuration	Note
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted	1 = *Normal Operation; No stall (iPU 3K) 0 = Stall	
CFG[1]	Reserved Configuration lane		
CFG[2]	PCI Express* Static x16 Lane Numbering Reversal	1 = *Normal Operation(iPU 3K) 0 = Lan number reversed	H & S processor used only
CFG[3]	Reserved Configuration lane		
CFG[4]	eDP enable	1 = Disabled (iPU 3K) 0 = *Enabled	
CFG[6:5]	PCI Express* Bifunction	00 = 1x8, 2x4 PCI Express* 01 = reserved 10 = 2x8 PCI Express* 11 = 1x16 PCI Express*	H & S processor used only
CFG[7]	PEG Training	1 = *PEG Train immediately follow RESET# de-assertion (iPU 3K) 0 = PEG wait for BIOS for training	H & S processor used only
CFG[19:8]	Reserved Configuration lane		



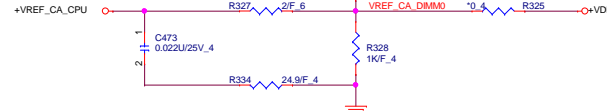
Skylake ULT (GND)





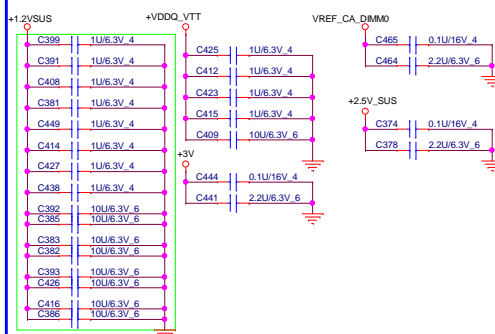


### VREF DQ0 M1 Solution

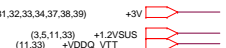


Place these Caps near So-Dimm1.

1uF/10uF 4pcs on each side of connector

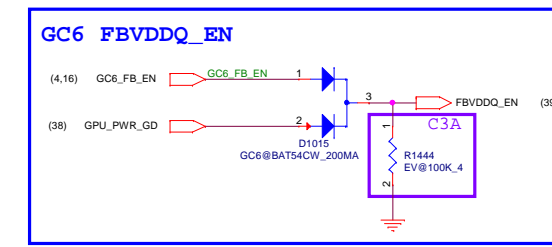




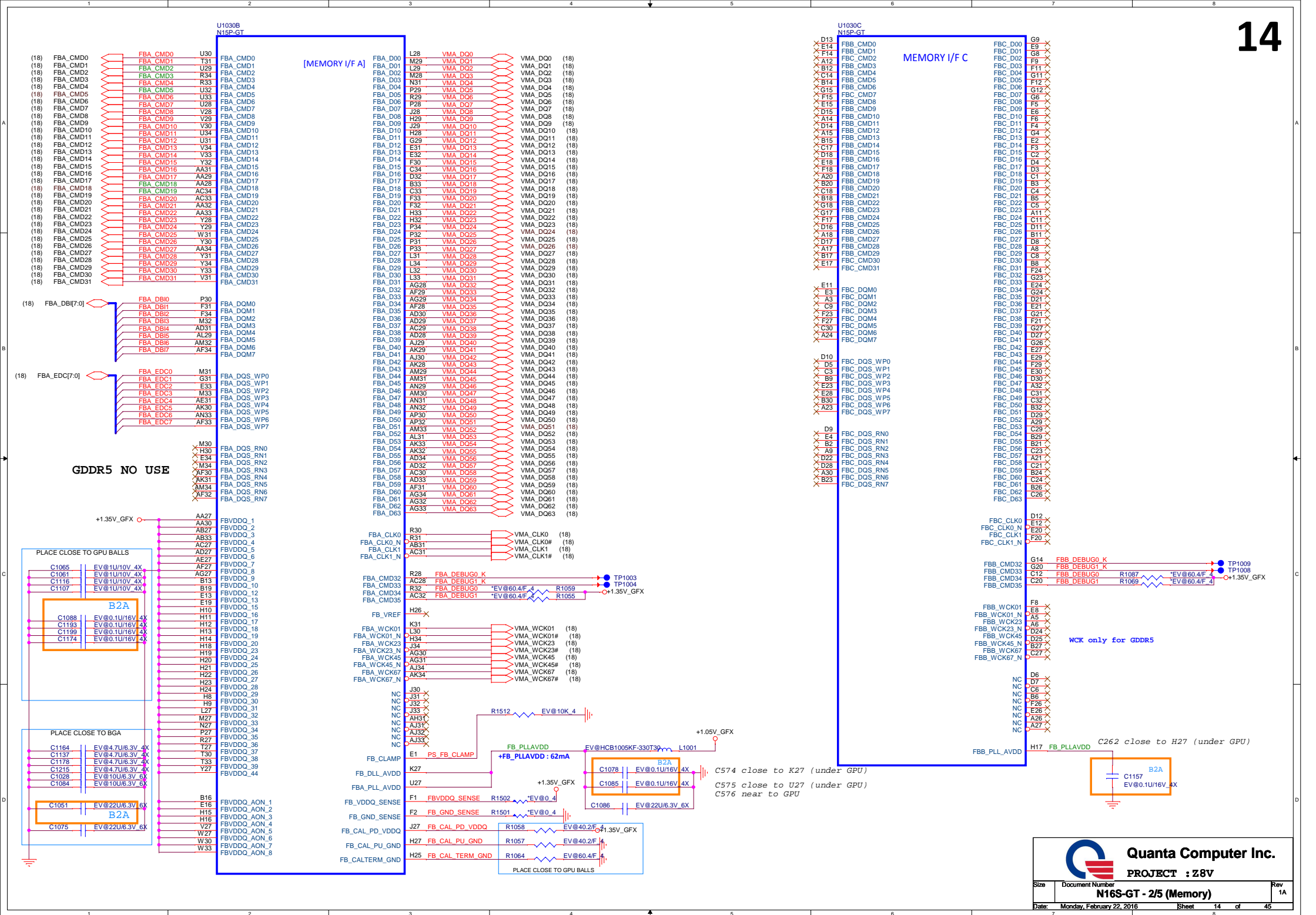


Size	Document Number	Rev
	<b>DDR4 DIMM-STD(5.2H) CHB</b>	1
Date:	Monday, February 22, 2016	Sheet 12 of 46

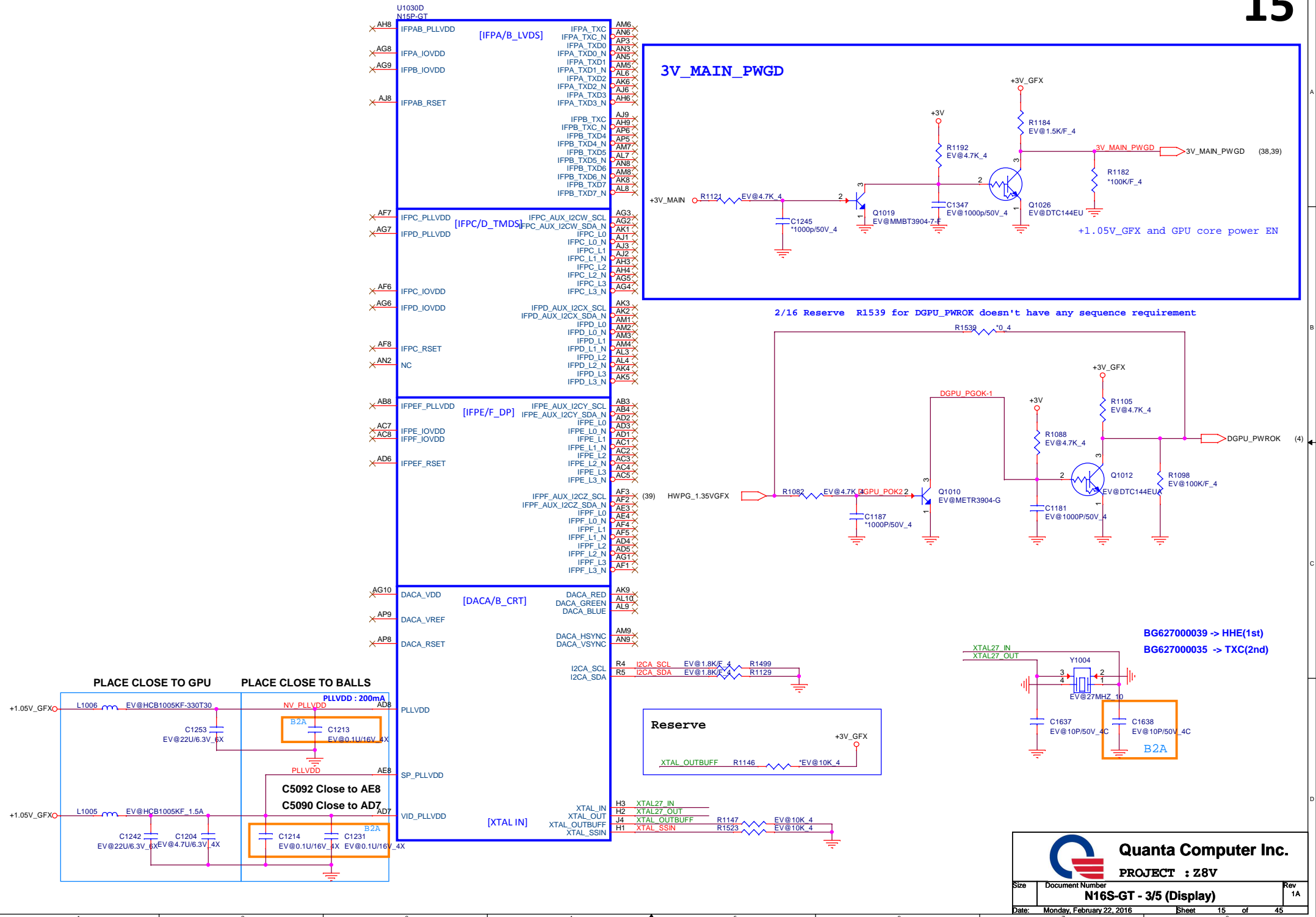














Package		DevID
N16S-GT1-KB	GB4b-128	0x179C
N16S-GTR	GB4b-128	0x134D

	PU +3V_MAIN	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

- Mutil-level mode strapping:

For N16S-GT1-KB-A2 :

R490=40.2k PD

1.ROM\_SCLK =4.99K PD

2.ROM\_SO = 4.99K PU (N16S-GTR = 4.99KPD)

3.ROM\_SI= Memory strap setting

4.STRAP0 = 49.9k PU  
5.Strap4~1 = Reserve Pull up and Pull down

	N16S-GT1-KB-A2	N16S-GTR
ROM_SO	R93 PU 4.99K	R92 PD 4.99K
ROM_SI	As below configuration table	

### N16S-GT1-KB-A2 VRAM Configuration Table:

	ROM_SI	DESCRIPTION	Vendor	Vendor P/N	STN P/N	ROM_SI
4GbX2 (1GB)	0011 (0x3) 0110 (0x6)	GGDR5 128MBx32 2500MHZ	SAMSUNG	K4G41325FC-HC03 --C die	AKG5PGDW2505	20K Pull down
		GGDR5 128MBx32 2500MHZ	HYNIX	H5GC42E4AJR-T2C --A die	AKG5PFWTW21	34.8K Pull down
4GbX4 (2GB)	0011 (0x3) 0110 (0x6)	GGDR5 256MBx16 2500MHZ	SAMSUNG	K4G41325FC-HC03 --C die	AKG5PGDW2505	20K Pull down
		GGDR5 256MBx16 2500MHZ	HYNIX	H5GC42E4AJR-T2C --A die	AKG5PFWTW21	34.8K Pull down
2GbX4 (2GB)	0000 (0x0) 0001 (0x3)	GGDR5 256MBx32 2500MHZ	SAMSUNG	AKG80325FB-HC03 --B die	AKG5QGDWT502	4.9K Pull up
		GGDR5 256MBx32 2500MHZ	MICRON	MT51J256G32HF-60:A--A die	AKG5GLUTL04	10K Pull up
4GbX4 (4GB)	0000 (0x0) 0001 (0x3)	GGDR5 512MBx16 2500MHZ	SAMSUNG	AKG80325FB-HC03 --B die	AKG5QGDWT502	4.9K Pull up
		GGDR5 512MBx16 2500MHZ	MICRON	MT51J256G32HF-60:A--A die	AKG5GLUTL04	10K Pull up

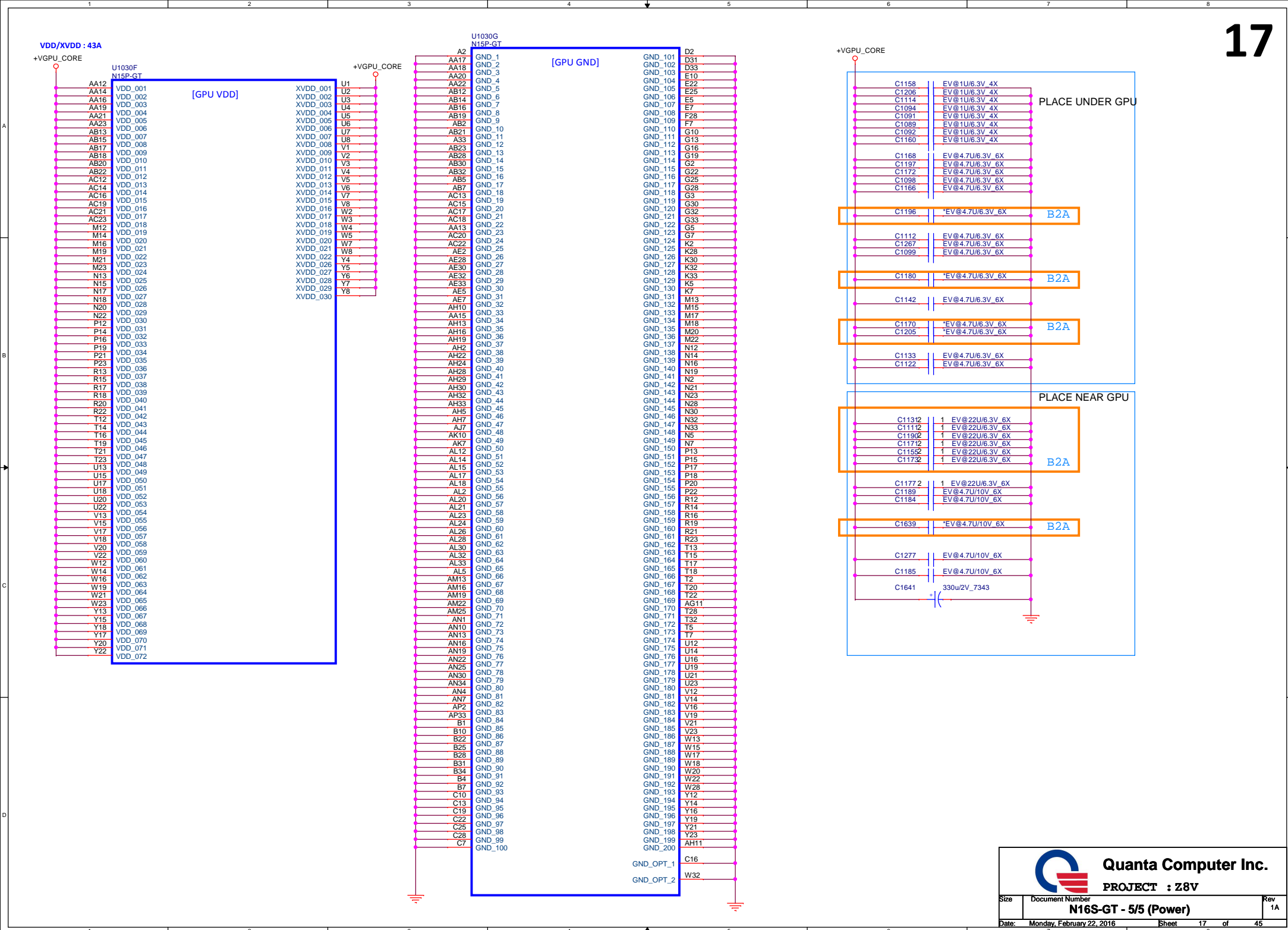
### N16S-GTR VRAM Configuration Table:

	ROM_Si	DESCRIPTION	Vendor	Vendor P/N	STN P/N	ROM_Si
4GbX2 (1GB)	0011 (0x3) 0110 (0x6)	GDDR5 128MBx32,2500MHz GDDR5 128MBx32,2500MHz	SAMSUNG HYNIX	K4G41325FC-HC03 --C die H5G44H24AJR-T2C --A die	AKG5PGDW21 AKG5PWTW21	20K Pull down 34.8K Pull down
4GbX4 (2GB)	0011 (0x3) 0110 (0x6)	GDDR5 256MBx16,2500MHz GDDR5 256MBx16,2500MHz	SAMSUNG HYNIX	K4G41325FC-HC03 --C die H5G44H24AJR-T2C --A die	AKG5PGDW21 AKG5PWTW21	20K Pull down 34.8K Pull down
8GbX2 (2GB)	0000 (0x0) 0001 (0x1)	GDDR5 256MBx32,2500MHz GDDR5 256MBx32,2500MHz	SAMSUNG MICRON	K4G80325FB-HC03 --B die MT51J256M32HF-60:A--A die	AKG5QDGT502 AKG5LGTU104	4.99K Pull down 10K Pull down
8GbX4 (4GB)	0000 (0x0) 0001 (0x1)	GDDR5 512MBx16,2500MHz GDDR5 512MBx16,2500MHz	SAMSUNG MICRON	K4G80325FB-HC03 --B die MT51J256M32HF-60:A--A die	AKG5QDGT502 AKG5LGTU104	4.99K Pull down 10K Pull down

N16S-GT1-KB-A2 (GB4b-128)

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	000
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXX
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE	000
STRAP0	Keep footprint to PU to 3V3_AON and PD to GND [Stuff 49.9K PU]				000
STRAP1	Keep footprint to PU to 3V3_AON and PD to GND [Do Not Stuff]				
STRAP2					
STRAP3					
STRAP4					







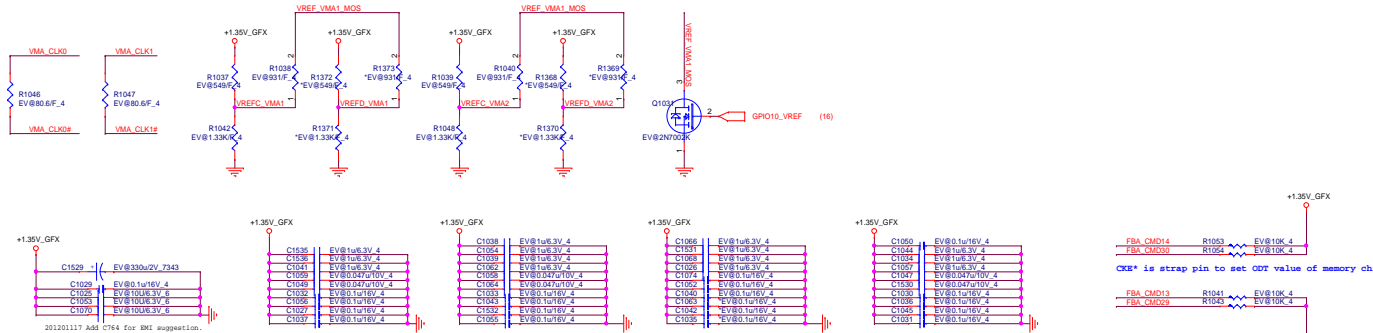
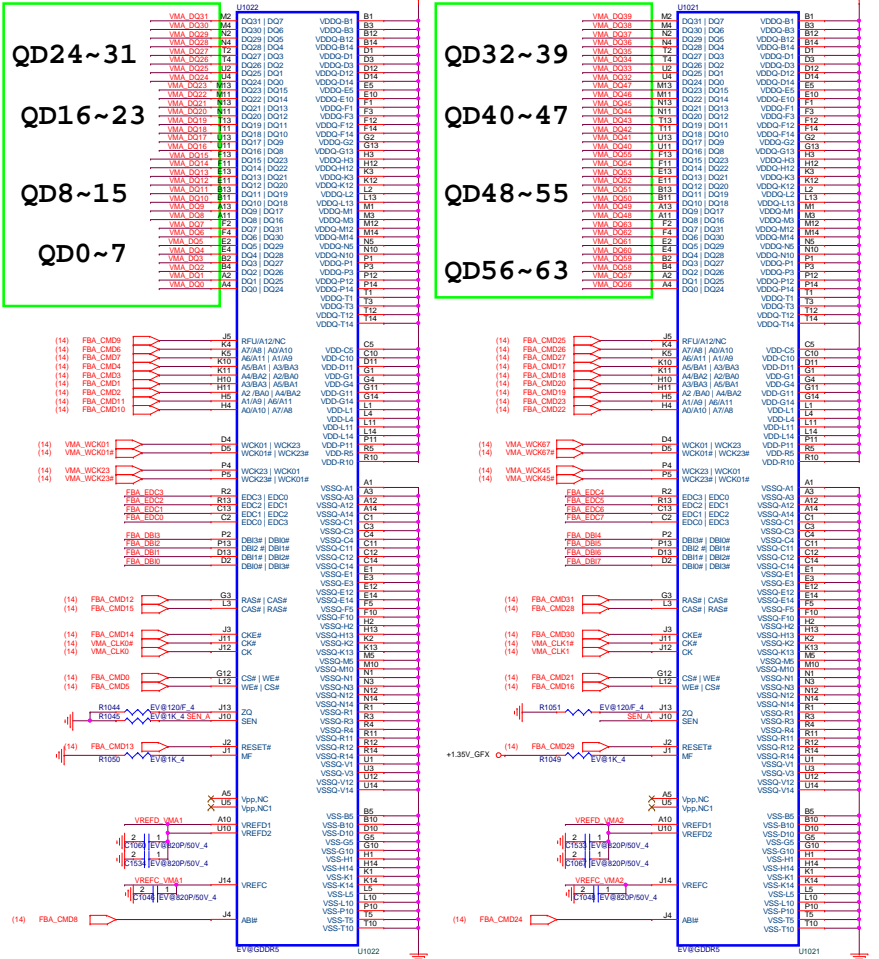
Channel 0  
<0-31>

LOWER HALF

Channel 0  
<32-63>

MF=0 Non-mirrored

MF=1 mirrored



## GDDR5 Mode II Mapping

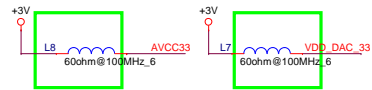
Channel	Bank	Memory
< 0-31 >	< 32-63 >	Memory
CM00	CM016	CSP*
CM01	CM017	A3_BA3
CM02	CM018	A2_BA2
CM03	CM019	A4_BA2
CM04	CM020	A5_BA1
CM05	CM021	WE*
CM06	CM022	A7_A8
CM07	CM023	A6_A11
CM08	CM024	AB1*
CM09	CM025	A12_BFT
CM10	CM026	A0_A10
CM11	CM027	A1_A9
CM12	CM028	RAS*
CM13	CM029	RST*
CM14	CM030	CKE*
CM15	CM031	CAS*

RST PD place @ the end of daisy-chain.

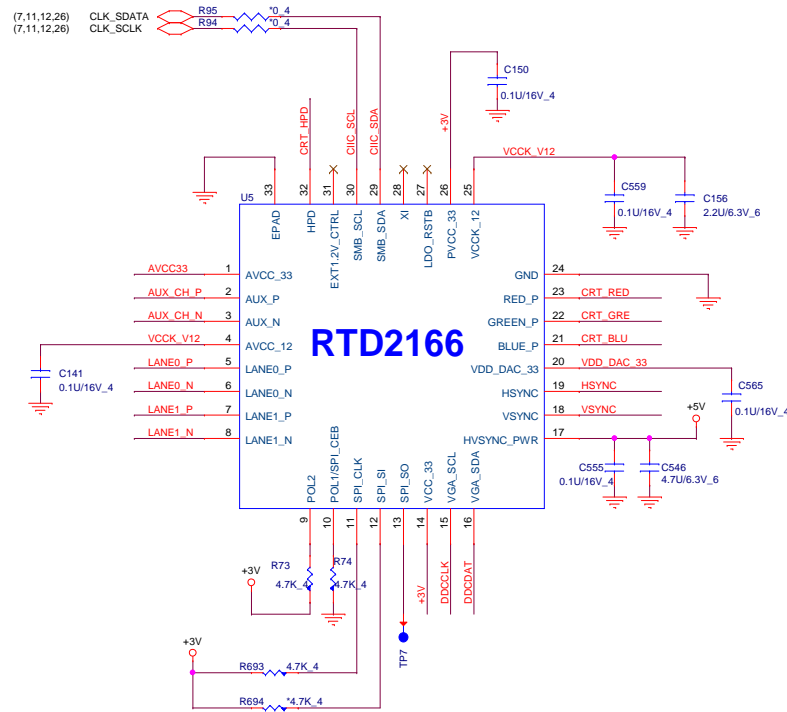
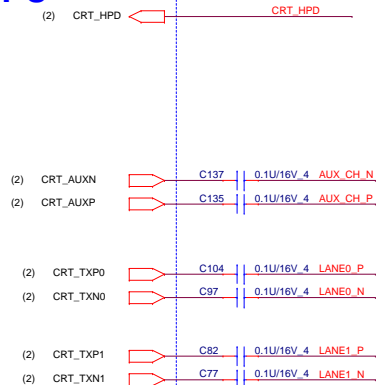


## DP TO VGA

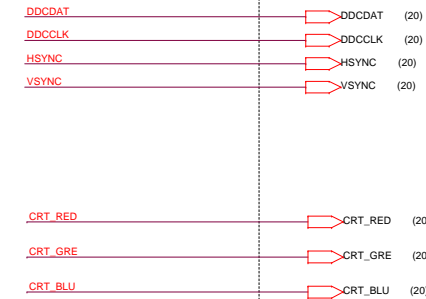
## Power



## CPU



## VGA

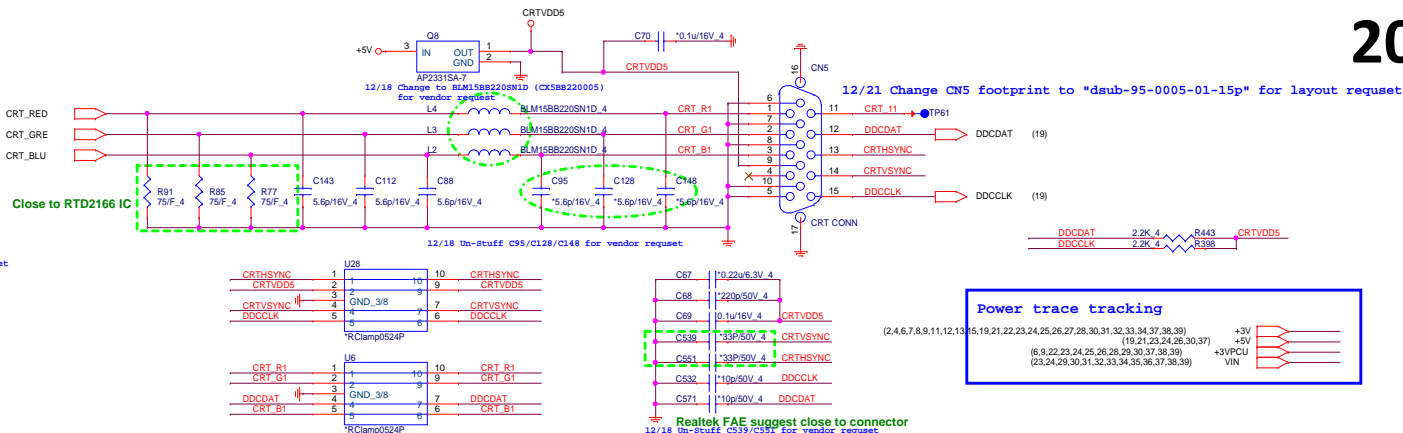


## Note:

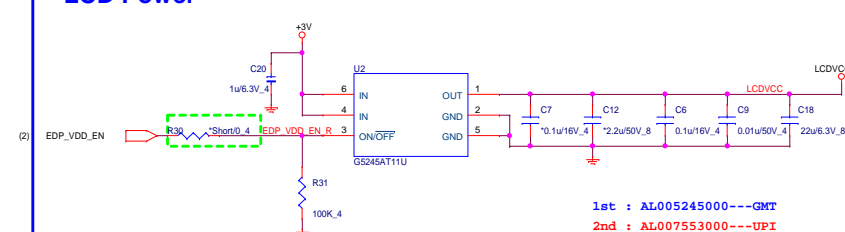
- 1- C1,C3,C4,C5,C11,C16, C21 should be placed close to chip
- 2- C5 should be X5R material
- 3- R6, R7, R8 should be 75 ohm with +/-1%
- 4- Suggest to connect Pin 29 and Pin 30 to PCH SMBUS for debug purpose.
- 5- This configuration is for internal ROM mode and using embedded LDO mode.

(2,4,6,7,8,9,11,12,13,15,20,21,22,23,24,25,26,27,28,30,31,32,33,34,37,38,39) +3V  
(20,21,23,24,26,30,37) +5V

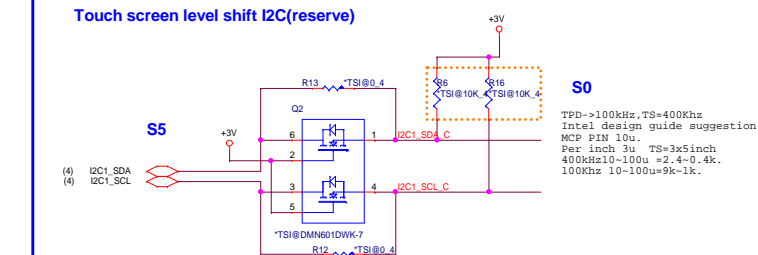




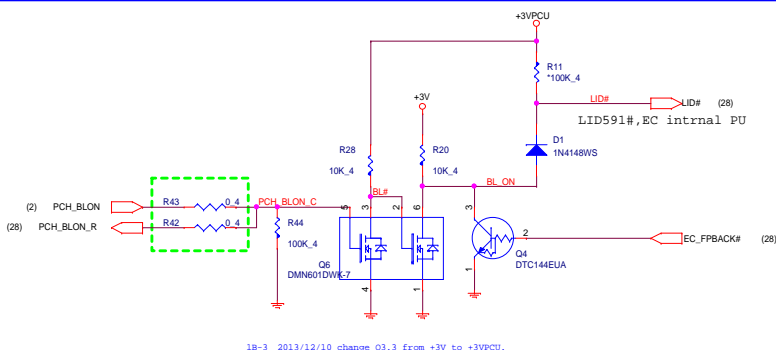
## LCD Power



**So**



1st:AL009249000 -- BCD  
2nd:AL009132001 -- ANC





HDMI <HDM>

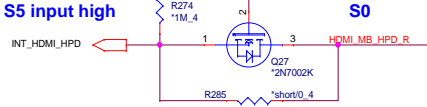
OE_N	DDC_EN	HPD_SINK	Source output	PTN3366 power mode
LOW	HIGH	HIGH	source active	Active mode; DDC active
LOW	LOW	LOW	don't care	Standby mode
HIGH	LOW	don't care	don't care	Ultra low-power mode

21

Inputs		Equalization for 3 Gbit/s
EQ1		
short to GND	short to GND	0 dB
short to GND	short to Vpp	2 dB
short to Vpp	short to GND	4 dB
short to Vpp	short to Vpp	6 dB

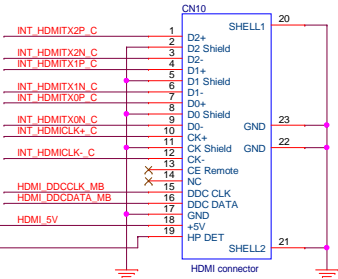
From PCH

HDMI-detect

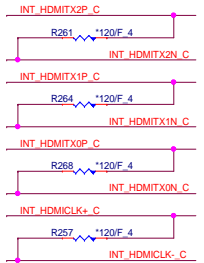


DDS AL002331000

HDMI connector

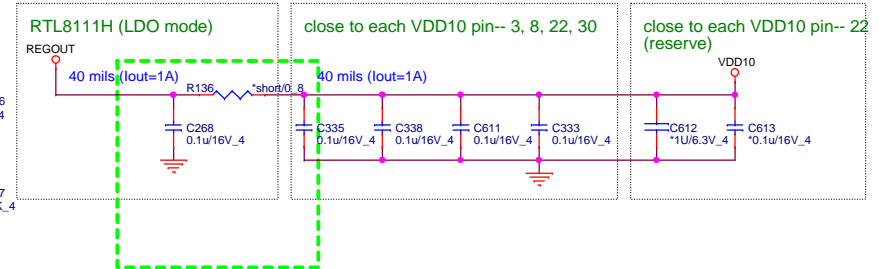
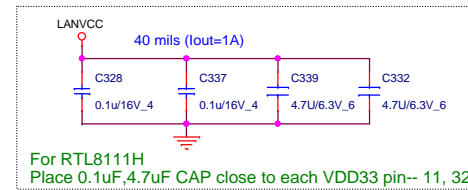
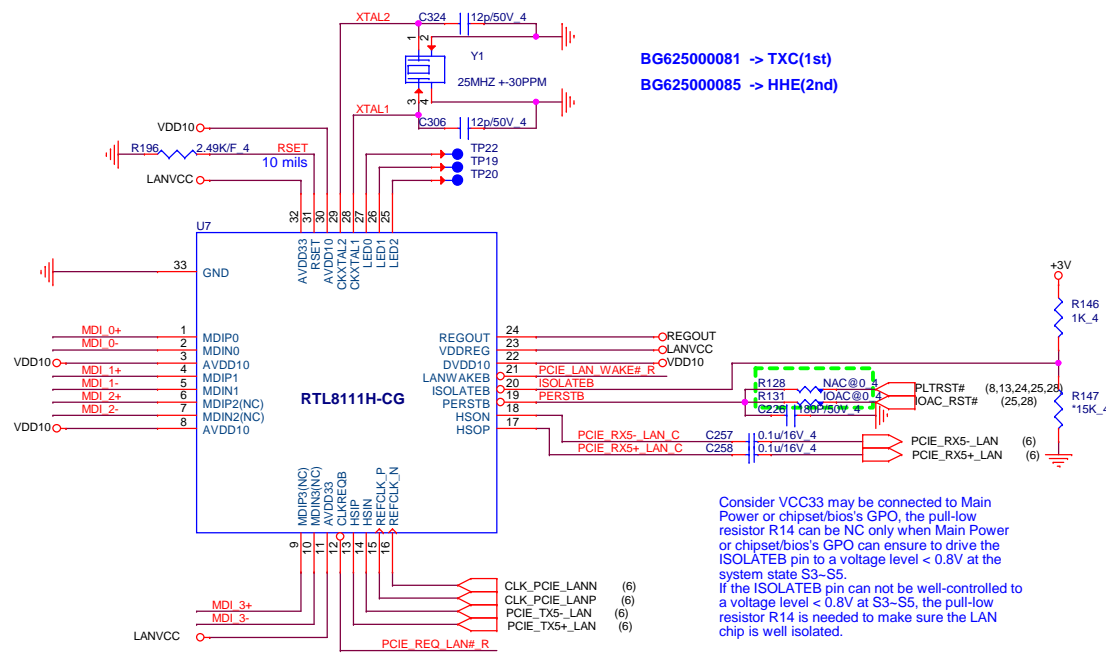


EMI

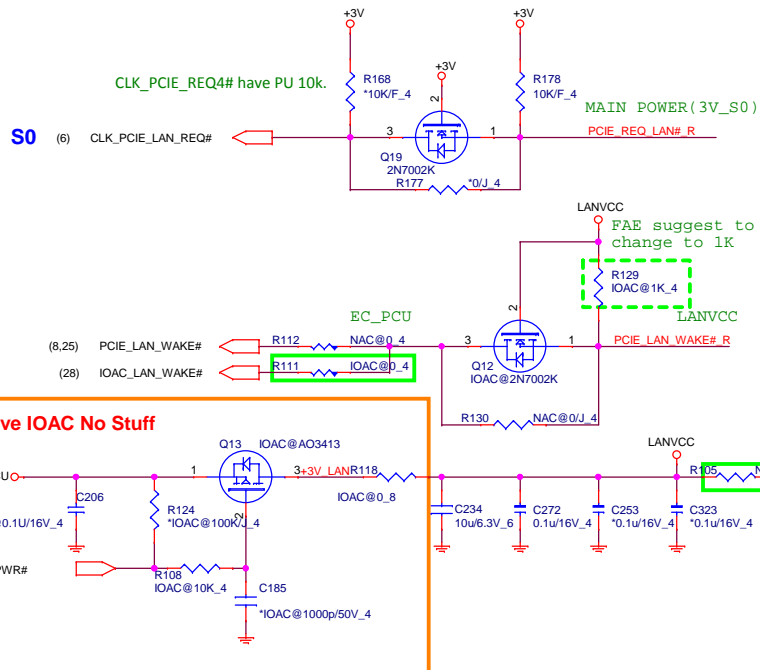


Power trace tracking



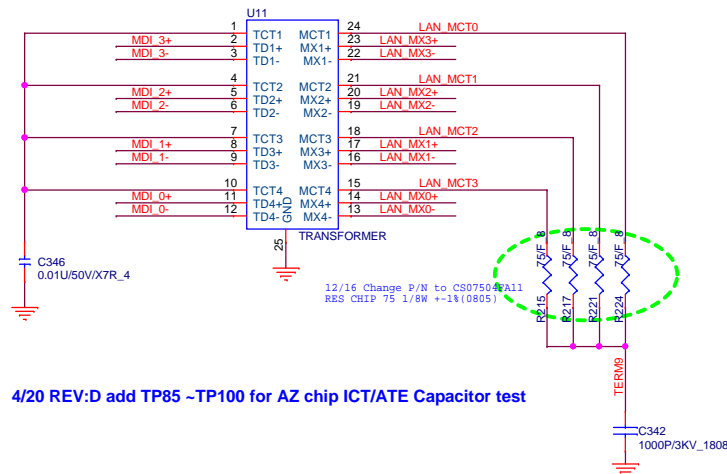


## Leakage circuit (MPC)

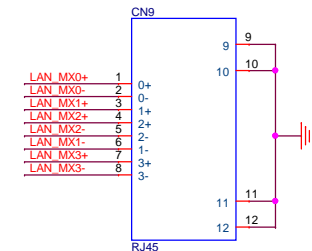


## Transformer

Layout: All termination signal should have 30 mil trace



## RJ45 Connector



**Quanta Computer Inc.**  
**PROJECT : ZRW**







20120921 change Cn10 Pin define following Z09.



24



## Reserve IOAC Power No Stuff

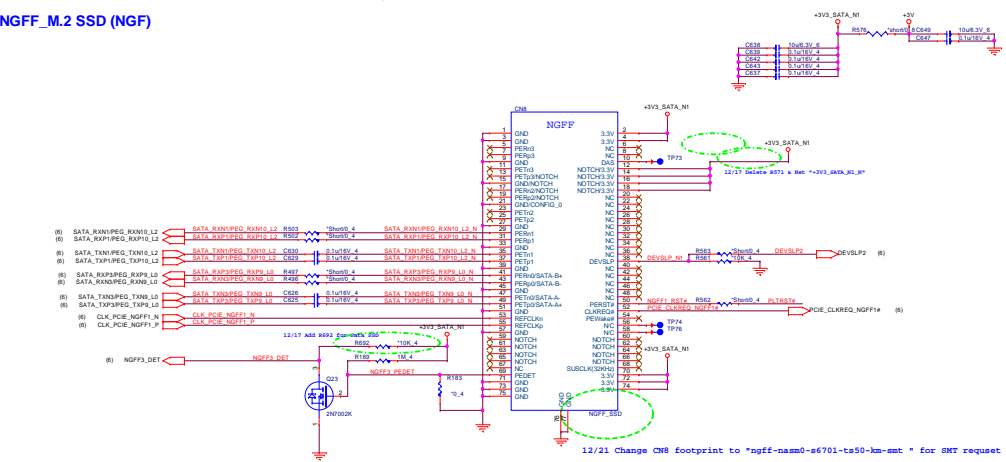
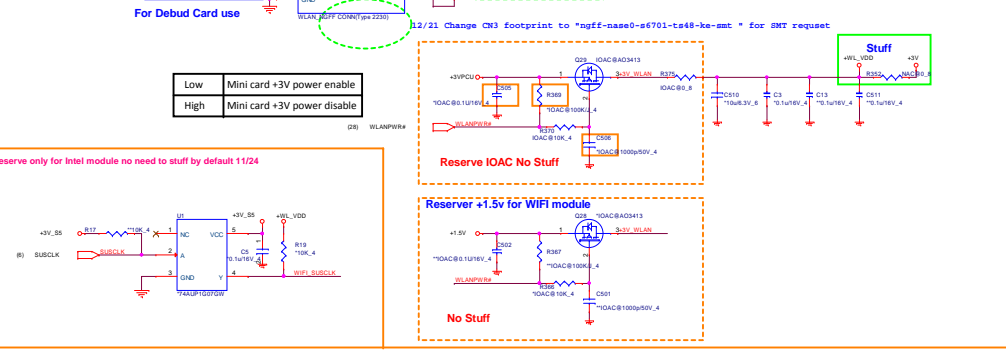
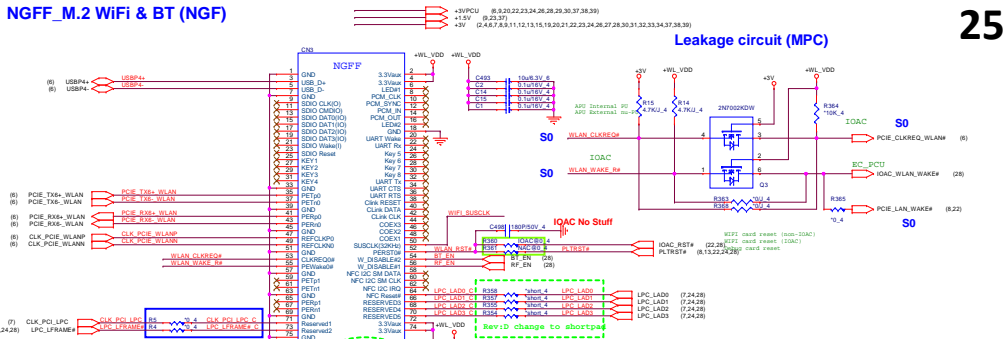


SP@ BOM周邊上NPCT650  
A,B,C P/N:AL009655K01(SLB9655TT1.2- FW4.31)  
RAMP P/N: AL000650K01 (NPCT650AAAWX)

TPMM 1.2	AL009655K01
TPMM 2.0	AL000650K01

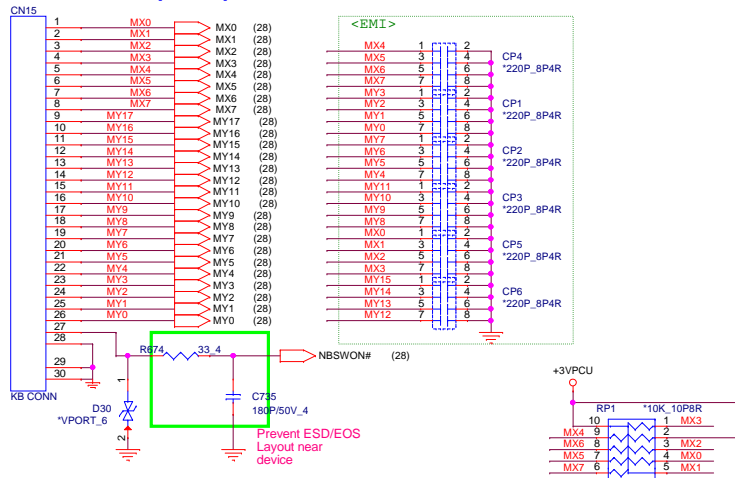




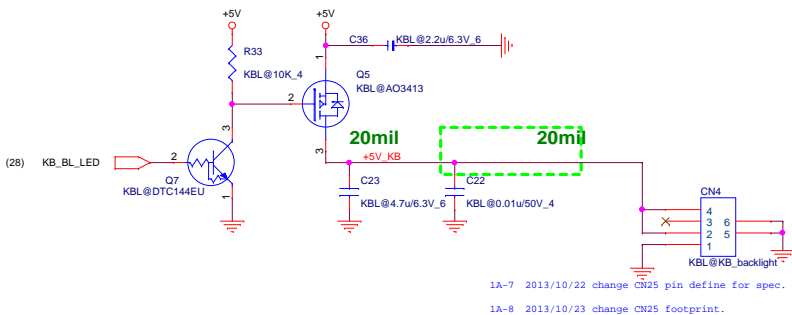




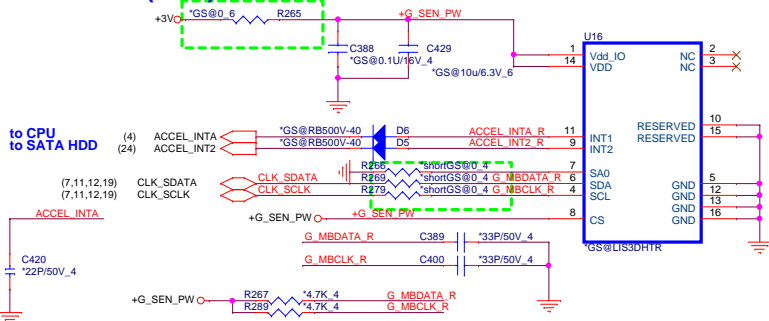
## KEYBOARD (KBC)



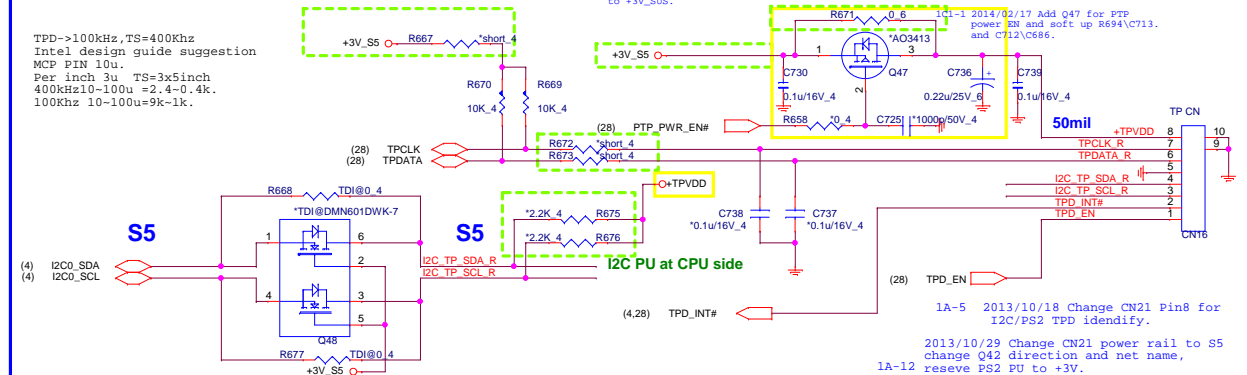
## KB\_LED (KBC)



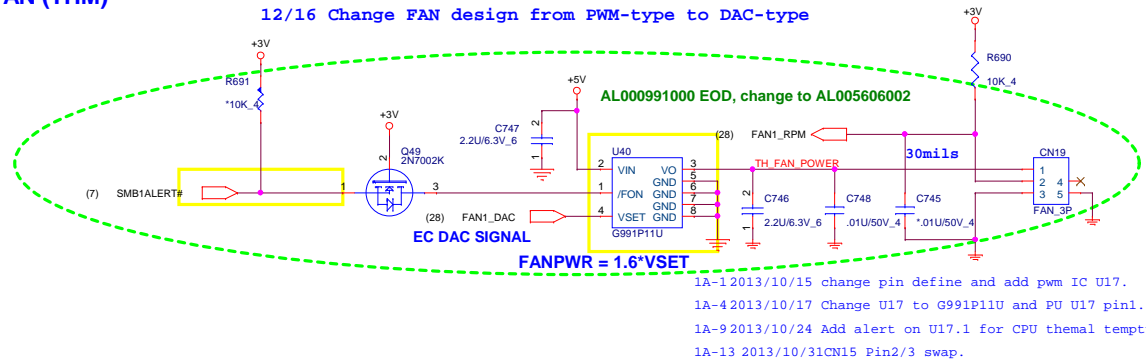
## G-sensor(ACS)



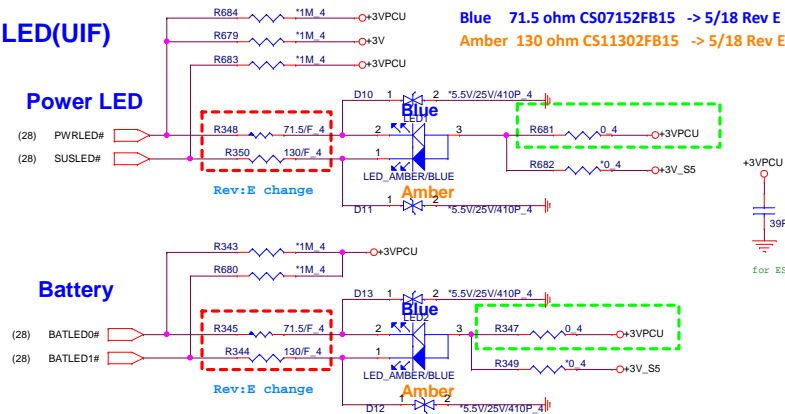
## TOUCHPAD BOARD CONN (TPD I2C/PS2 co-lay)



## CPU FAN (THM)



## POWER LED(UIF)





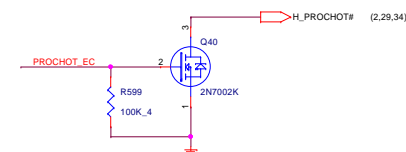




## 28

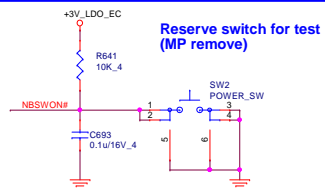
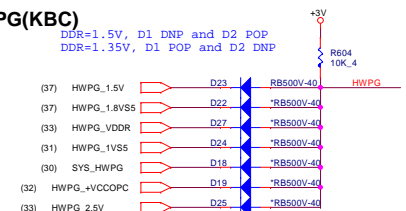


UMA& VGA SK  
Need Stuff



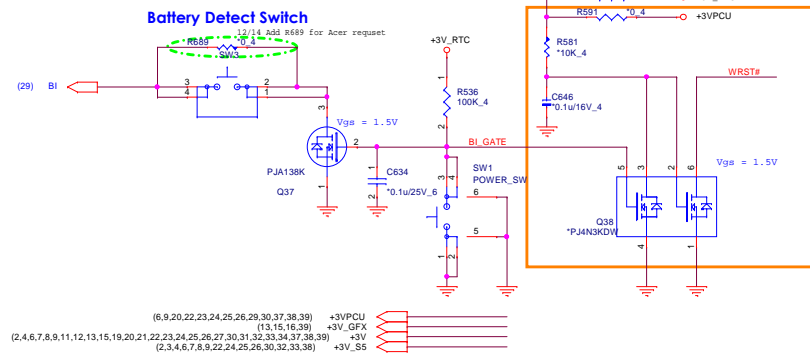
## HWPG(KBC)

DDR=1.5V, D1 DNP and D2 POP  
DDR=1.35V, D1 POP and D2 DNP



## Reset SW (FSW)

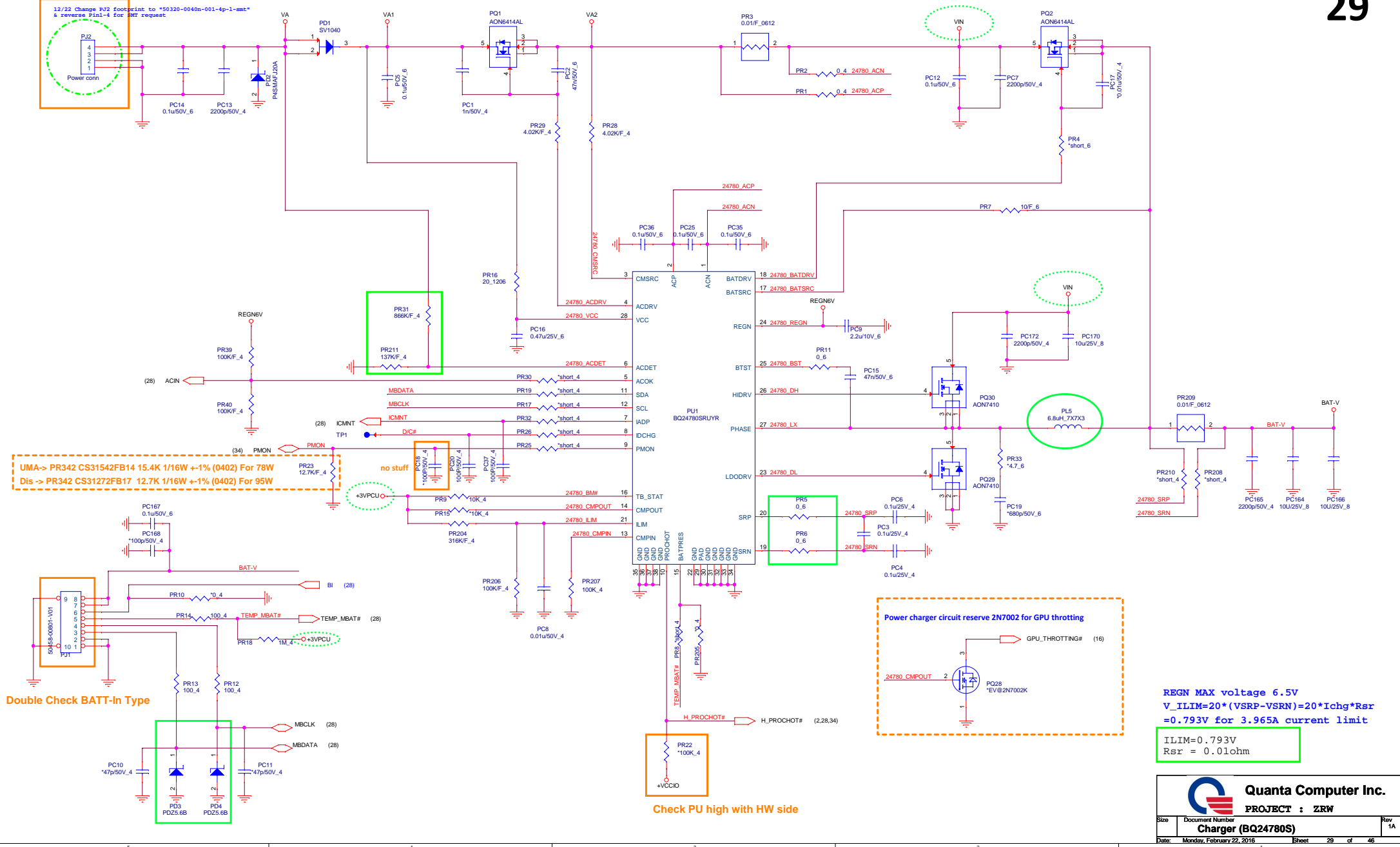
## Battery Detect Switch



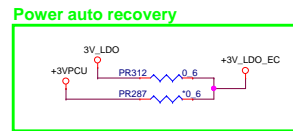
- Reserve no stuff



## Double Check ADP-In Type





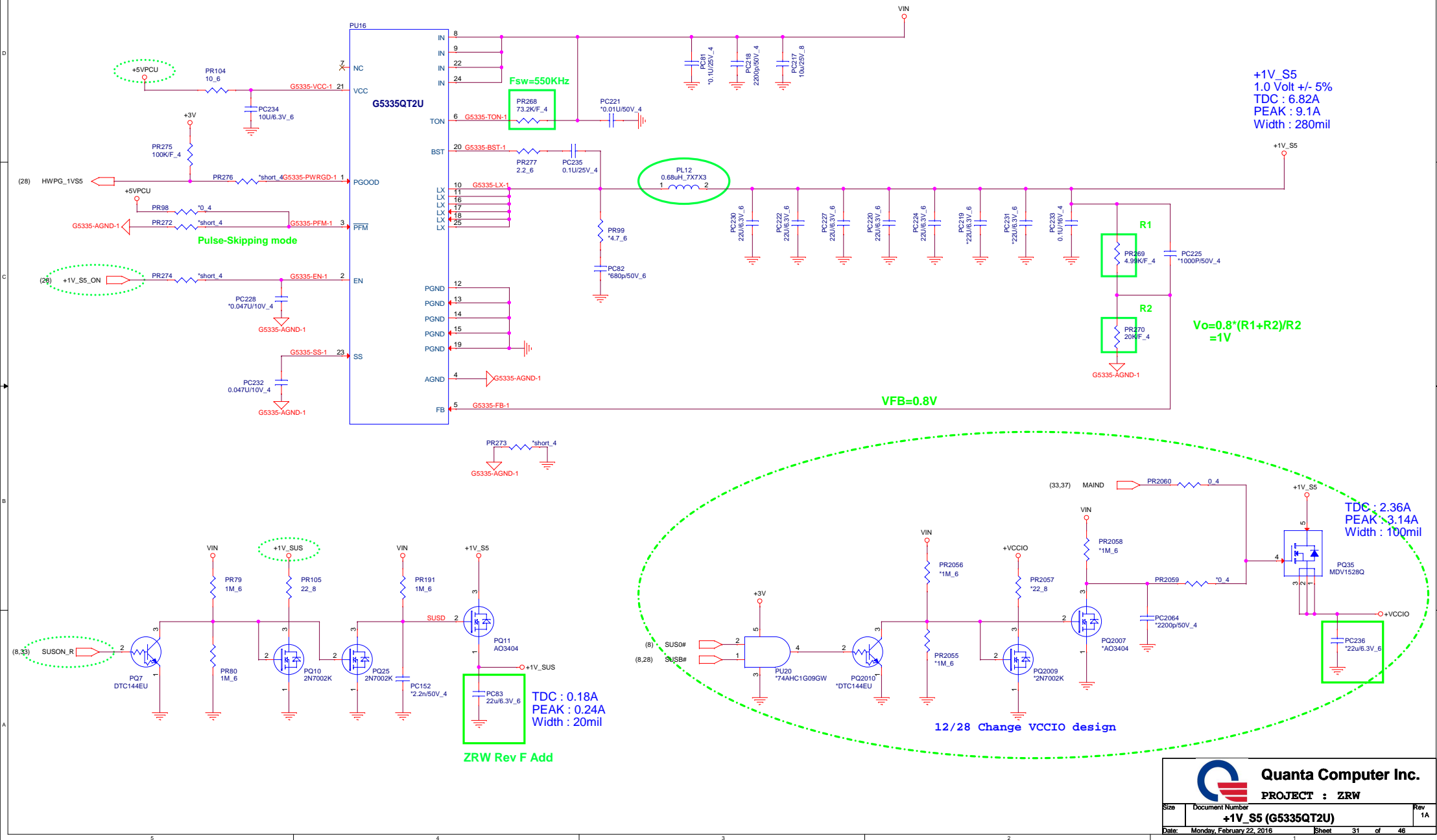


$L(\text{ripple current}) = (9-5) \cdot 5 / (2.2 \cdot 0.3 \cdot 9) = 3.367 \text{ A}$   
 $I_{\text{ocp}} = 12 - (3.367/2) = 10.316 \text{ A}$   
 $V_{\text{th}} = (10.316 \text{ A} \cdot 14.5 \text{ m}\Omega) + 1 \text{ mV} = 150.589 \text{ mV}$   
 $R(I_{\text{lim}}) = (150.589 \text{ mV} \cdot 8) / 10 \text{ uA} \sim 120.47 \text{ K}$

$L(\text{ripple current}) = (9-3.3) \cdot 3.3 / (2.2 \mu \cdot 0.355 \text{M} \cdot 9) \approx 2.676 \text{A}$   
 $I_{\text{ocp}} = 10 - (2.676/2) = 8.662 \text{A}$   
 $V_{\text{th}} = (8.662 \text{A} \cdot 14.5 \text{m}\Omega) + 1 \text{mV} = 126.599 \text{mV}$   
 $R(\text{Ilim}) = (126.599 \text{mV} \cdot 8) / 10 \mu \text{A} = 101.279 \text{K}$







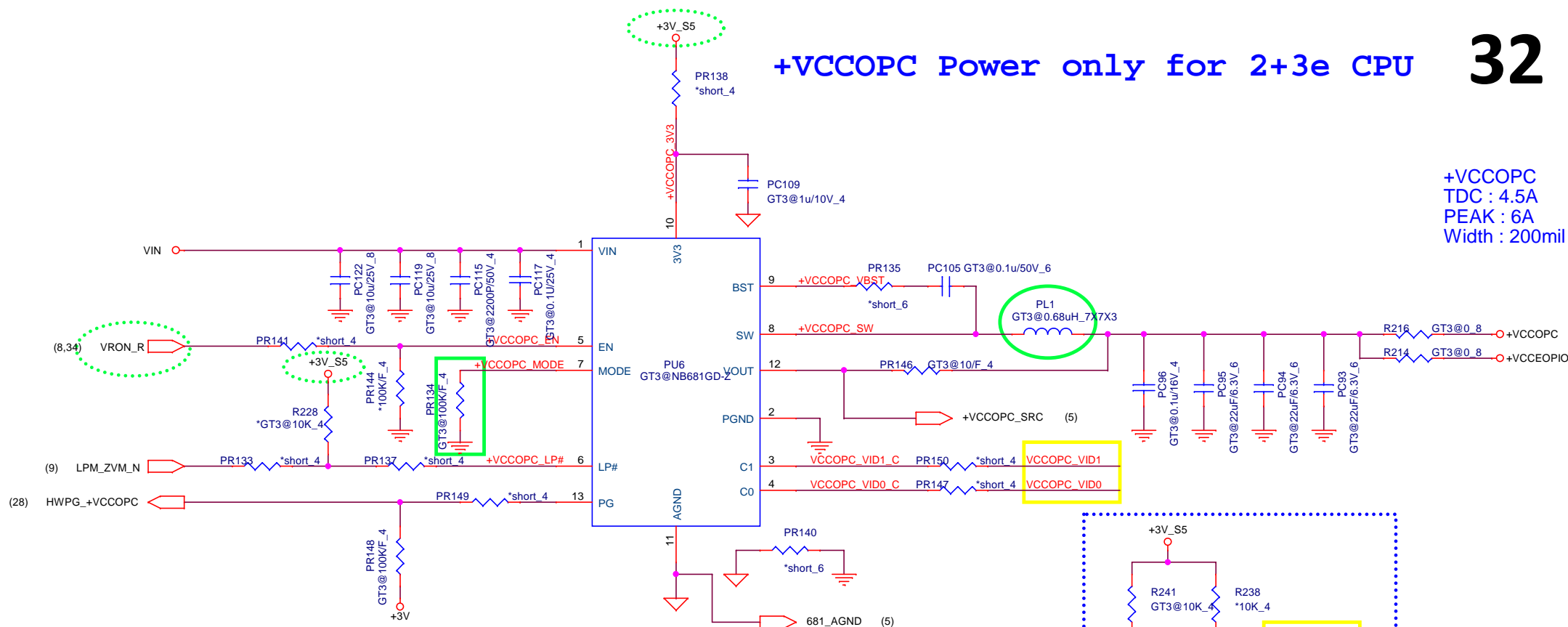
**Quanta Computer Inc.**  
PROJECT : ZRW

Size Document Number Rev 1A  
+1V\_S5 (G5335QT2U)  
Date: Monday, February 22, 2016 Sheet 31 of 46



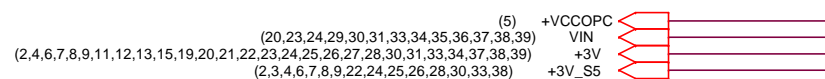
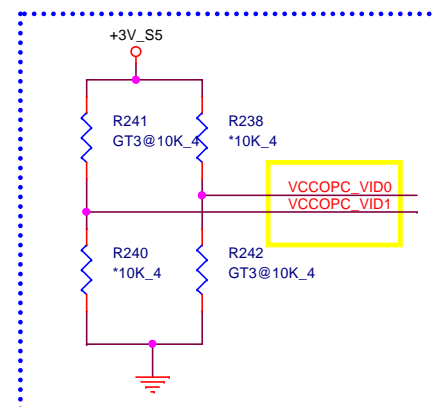
**+VCCOPC Power only for 2+3e CPU**

+VCCOPC  
TDC : 4.5A  
PEAK : 6A  
Width : 200mil

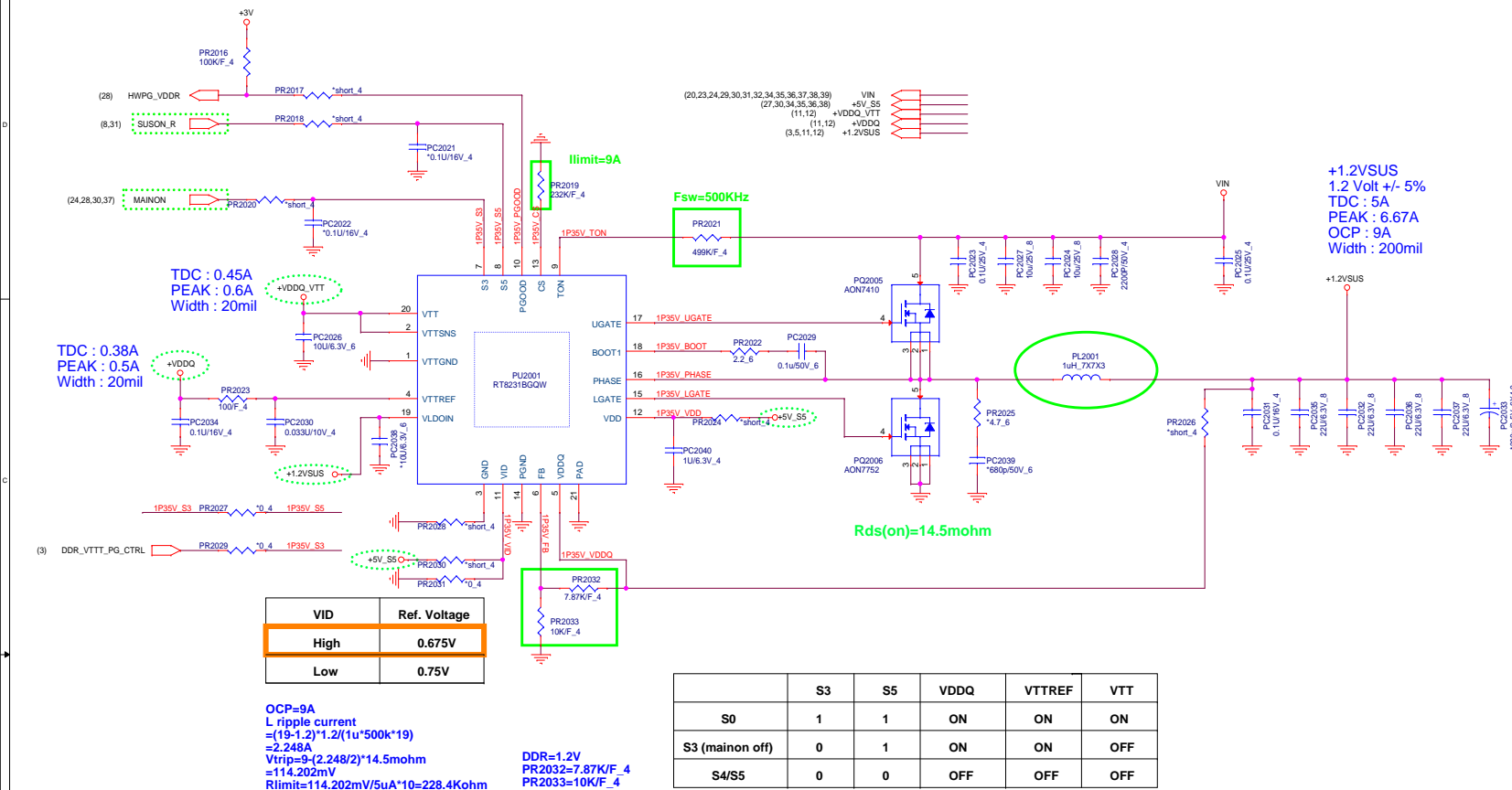


Mode	VR Rail
0 ohm	VCCIO
Floating	PRIMCORE
100K	EDRAM/EOPIO
150K	Other

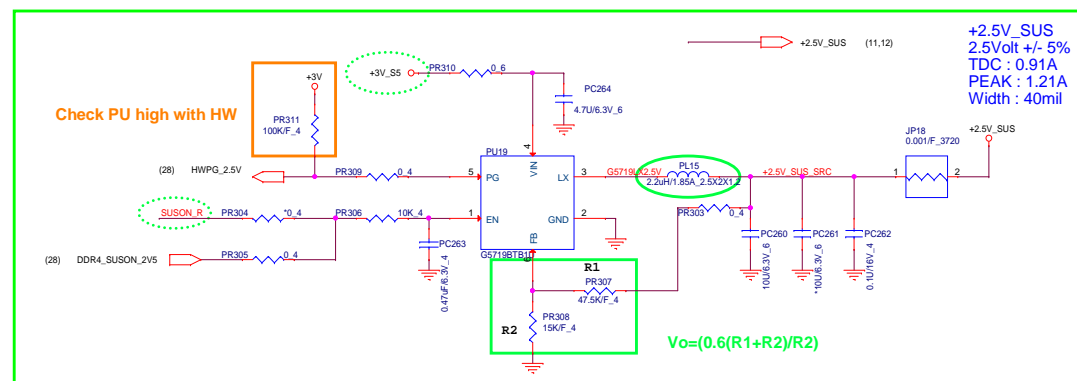
	LP#	C1	C0	Vo
<b>VCCEDRAM</b>	0	X	X	0V
	1	0	0	0.8V(MSM
	1	0	1	0.95V
	1	1	0	1.0V
	1	1	1	1.05V



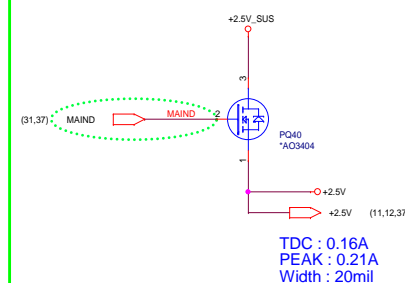




## +2.5VSUS Power Rail For DDR4

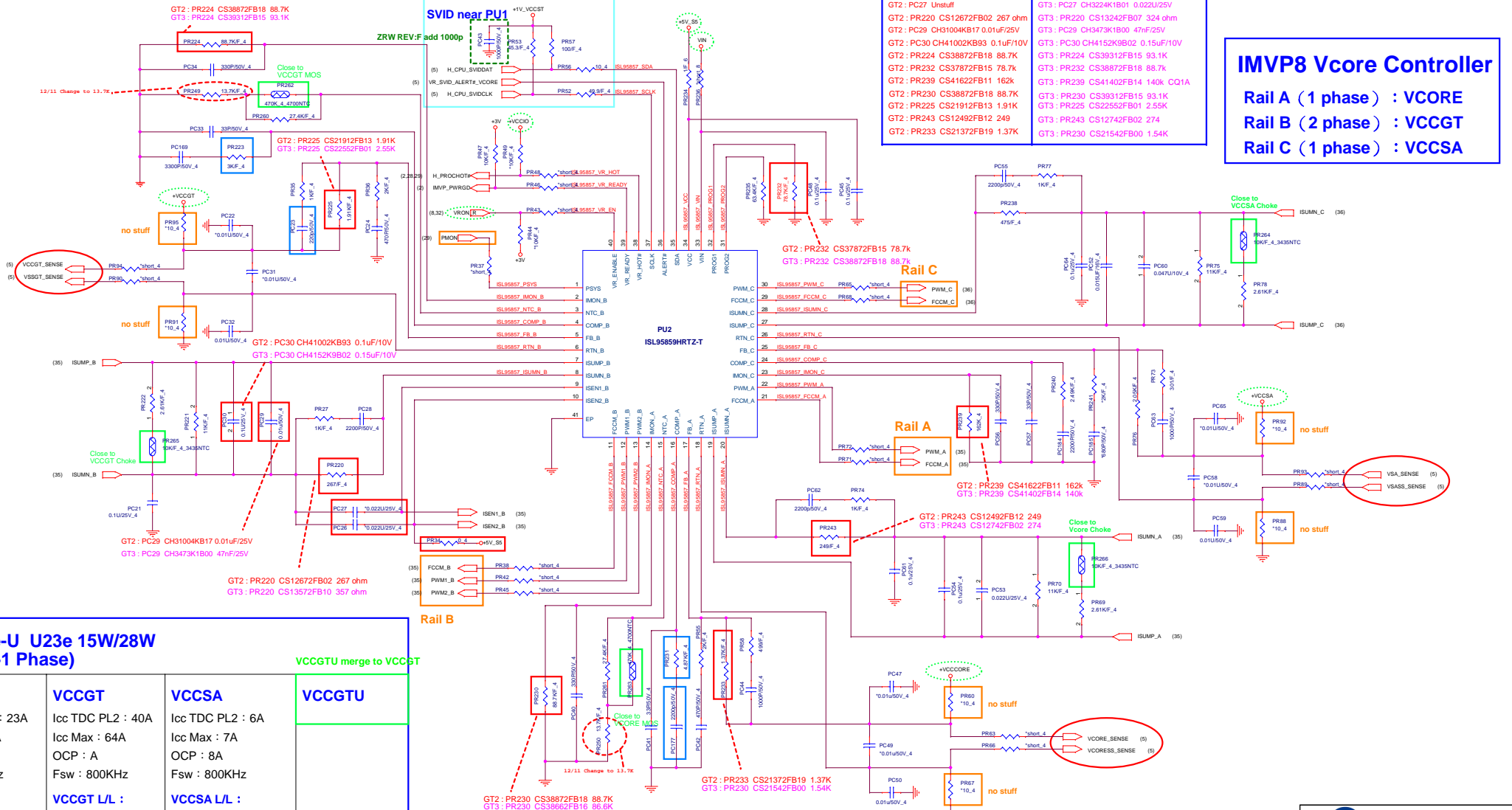


## 10/26 Reserve +2.5V for DDR4 VDDSPD





Check PU high with HW

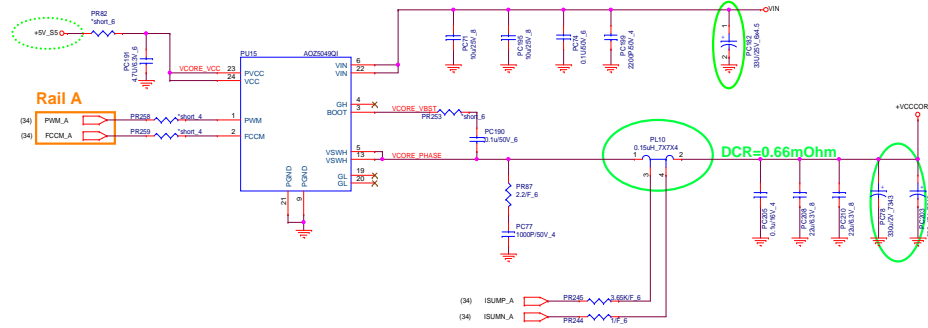




GT2: PR19 Unstuff

GT3: PR19 CS41003F932 100K

## VCORE



## VCORE

Icc TDC PL2 : 23A

Icc Max : 29A

OCP : 35A

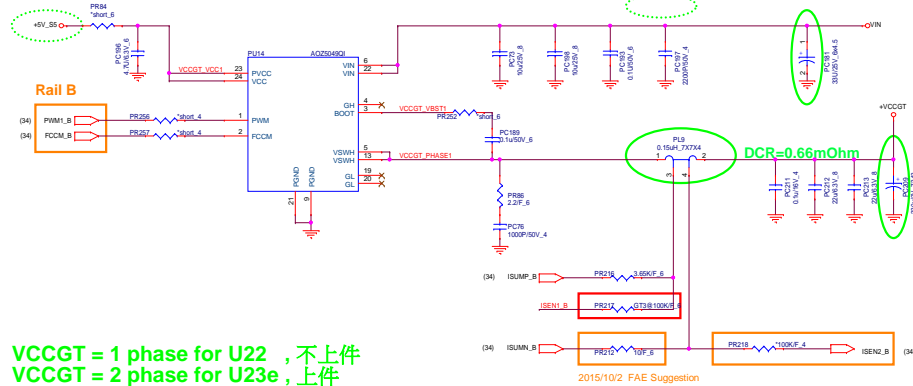
Fsw : 800KHz

## VCORE L/L :

R\_DC\_LL : 2.1mV/A

R\_AC\_LL : 2.1mV/A

## VCCGT



## VCCGT

Icc TDC PL2 : 40A

Icc Max : 64A

OCP : A

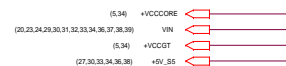
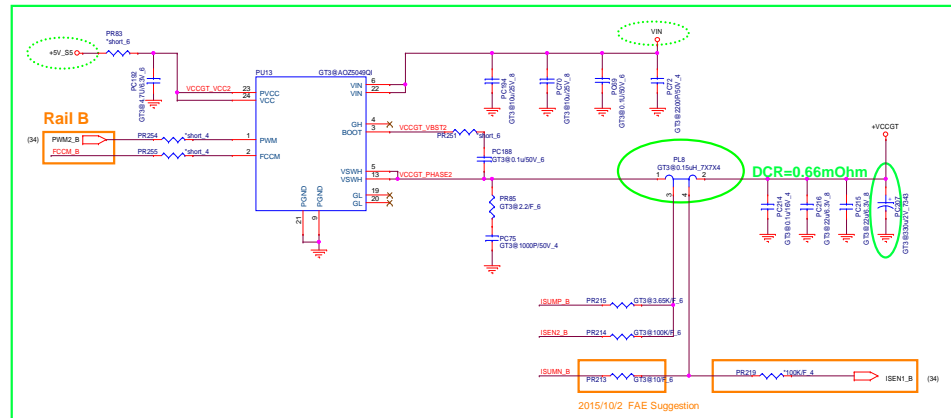
Fsw : 800KHz

## VCCGT L/L :

R\_DC\_LL : 2mV/A

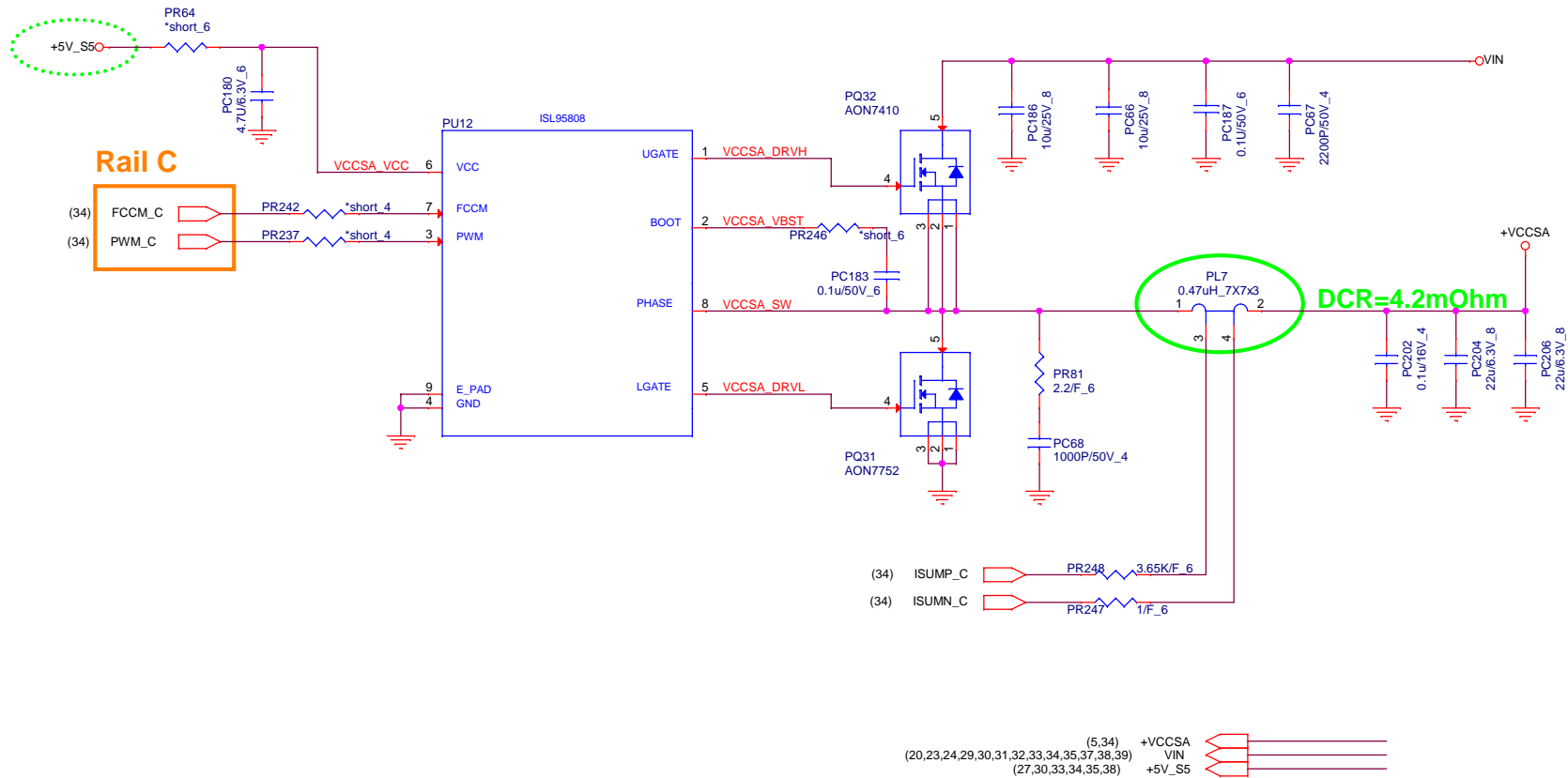
R\_AC\_LL : 2mV/A

VCCGT = 1 phase for U22 , 不上件  
 VCCGT = 2 phase for U23e , 上件





# VCCSA



## VCCSA

Icc TDC PL2 : 5A

Icc Max : 5A

OCF : 6A

Fsw : 800KHz

VCCSA L/L :

R\_DC\_LL : 10.3mV/A

R\_AC\_LL : 10.3mV/A



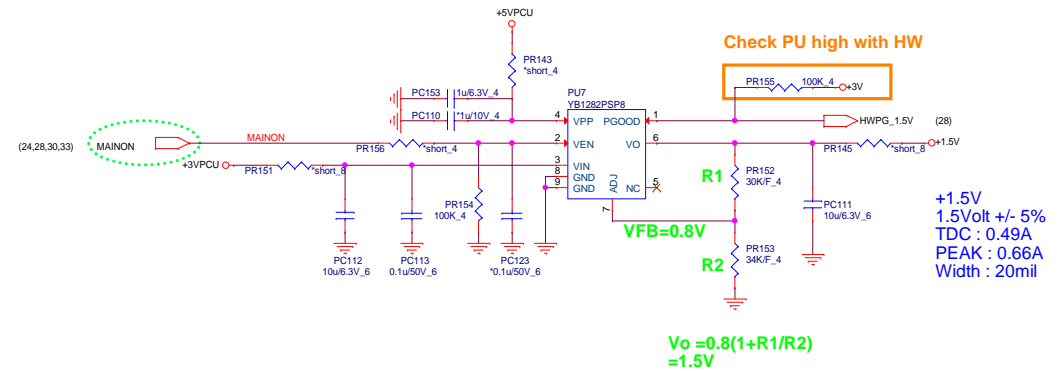
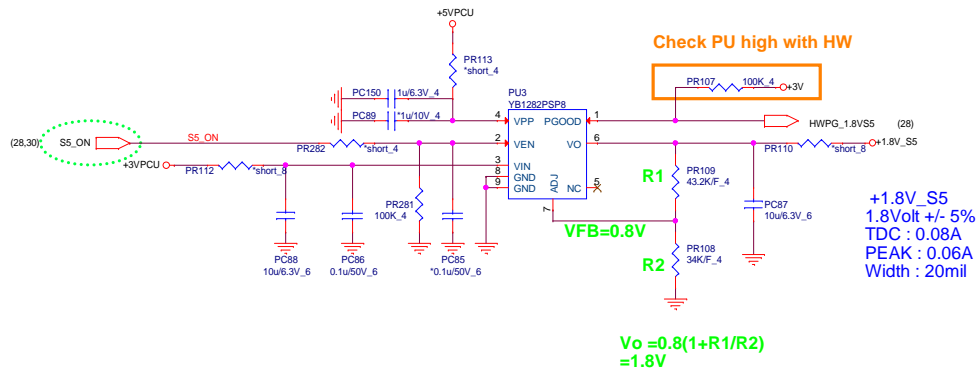
**Quanta Computer Inc.**

**PROJECT : ZRW**

Size	Document Number	Rev
	<b>VCCSA (ISL95808HRZ-T)</b>	1A

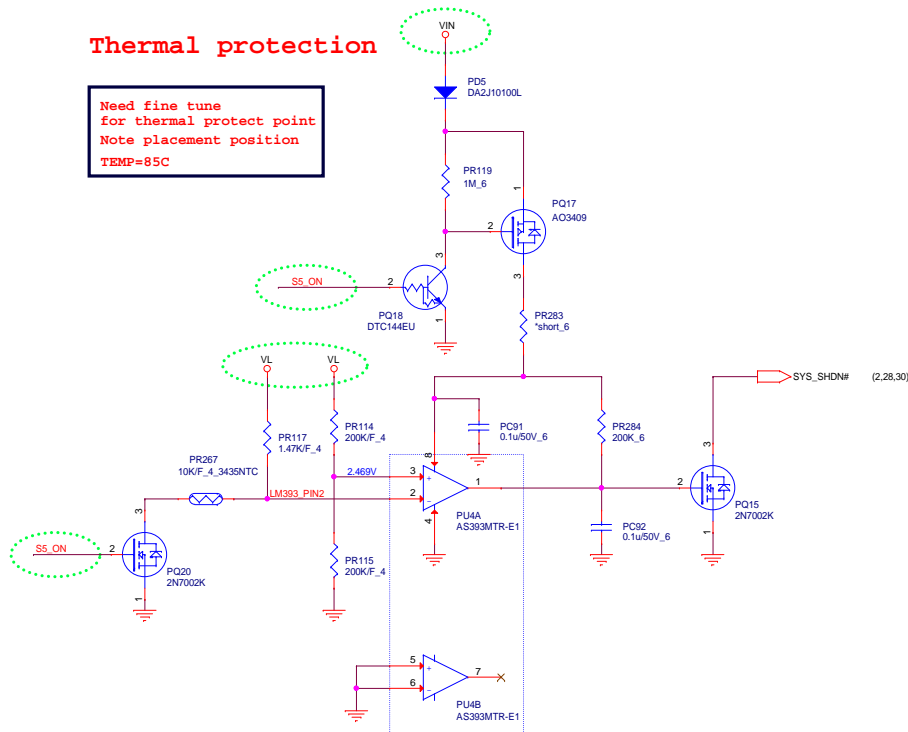
Date: Monday, February 22, 2016 Sheet 36 of 46



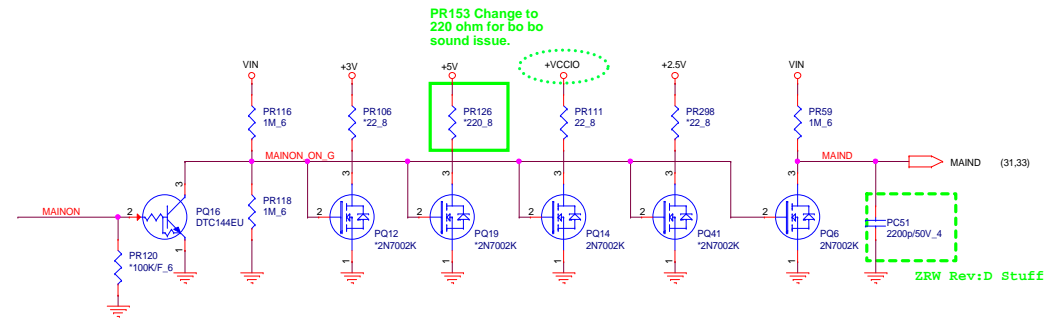


### Thermal protection

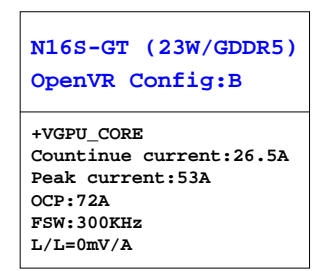
Need fine tune  
for thermal protect point  
Note placement position  
TEMP=85C



For EC control thermal protection (output 3.3V)



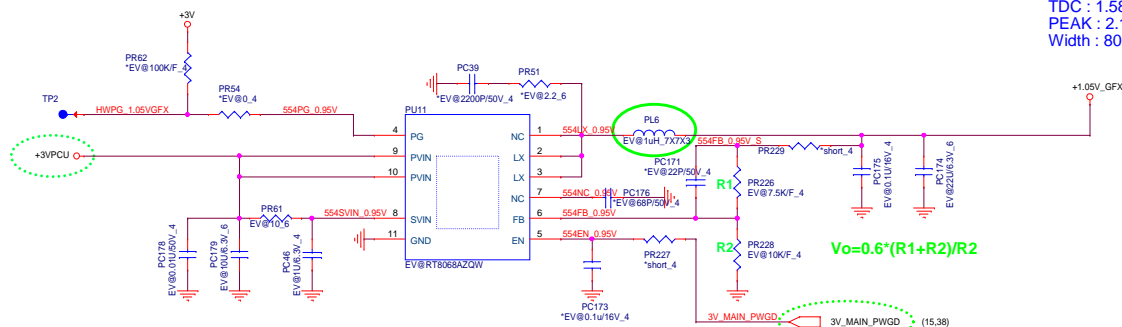




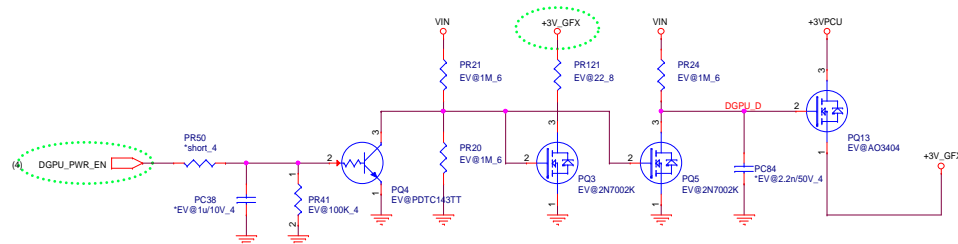


(13,14,15) +1.05V\_GFX  
(13,15,16,29) +3V\_GFX  
(14,16) +1.35V\_GFX

+1.05V\_GFX  
TDC : 1.58A  
PEAK : 2.1A  
Width : 80mil

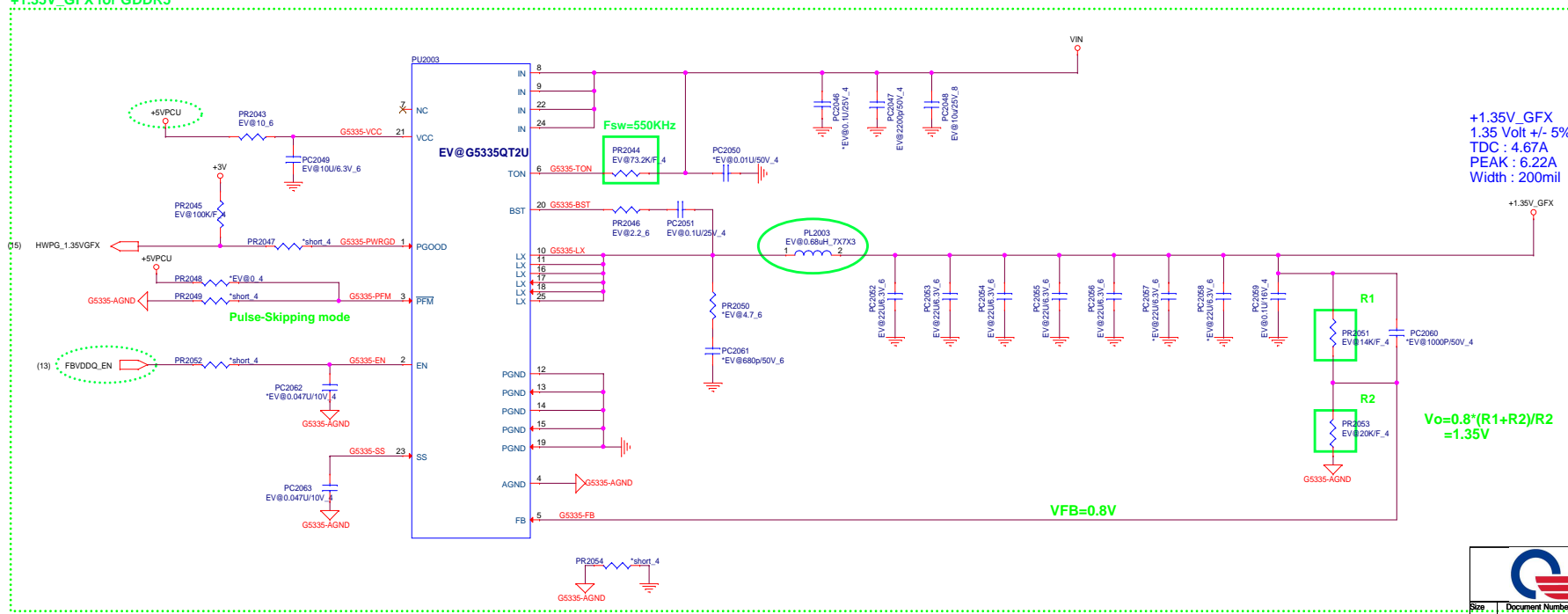


$$V_o = 0.6 * (R1 + R2) / R2$$



+3V\_GFX  
TDC : 0.05A  
PEAK : 0.06A  
Width : 20mil

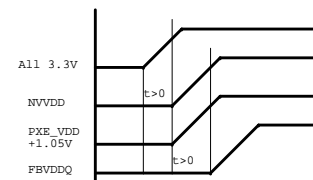
+1.35V\_GFX for GDDR5



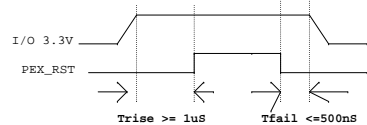
+1.35V\_GFX  
1.35 Volt +/- 5%  
TDC : 4.67A  
PEAK : 6.22A  
Width : 200mil

$$V_o = 0.8 * (R1 + R2) / R2 = 1.35V$$





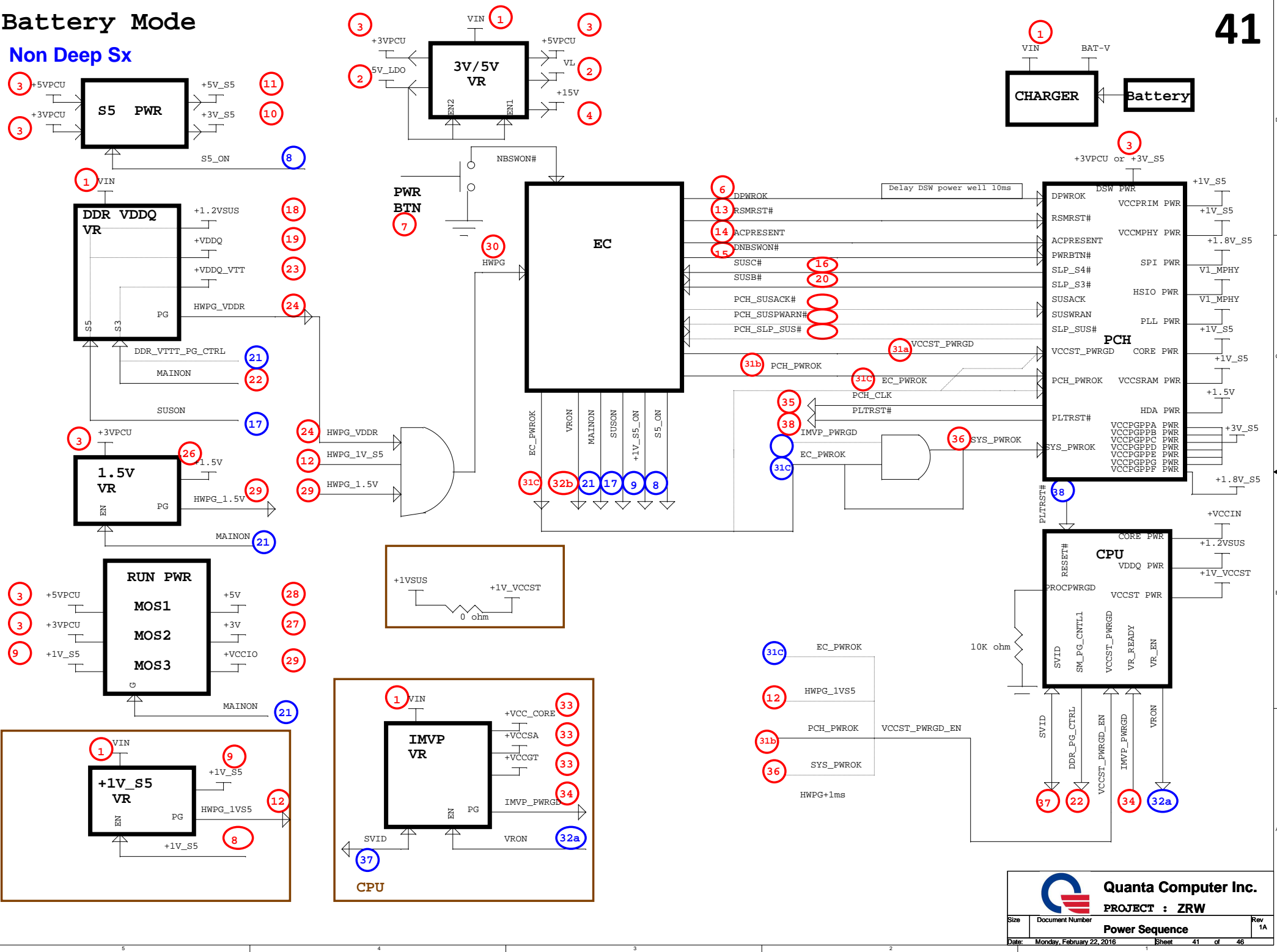
### VGA Reset





Battery Mode

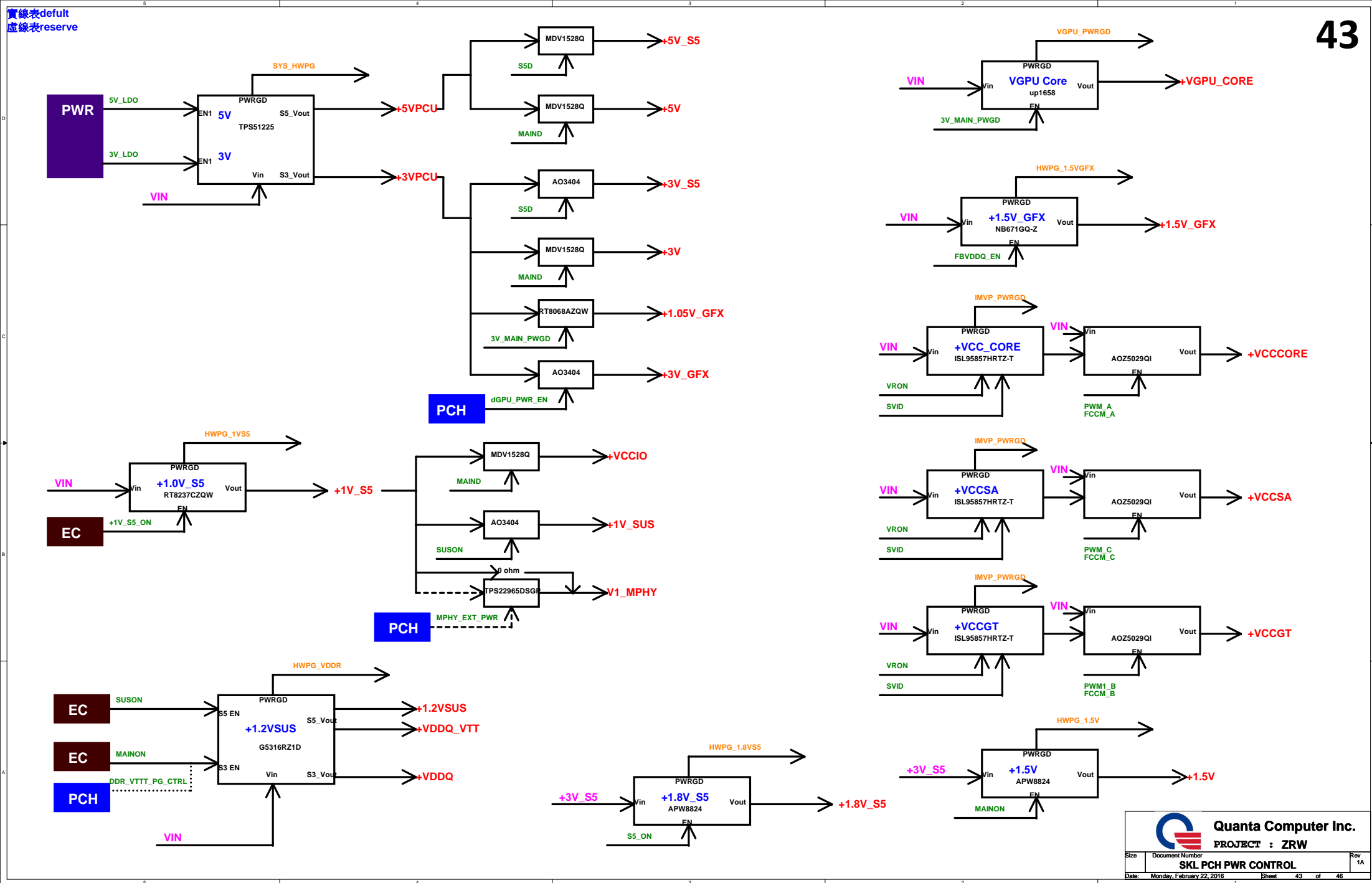
Non Deep Sx





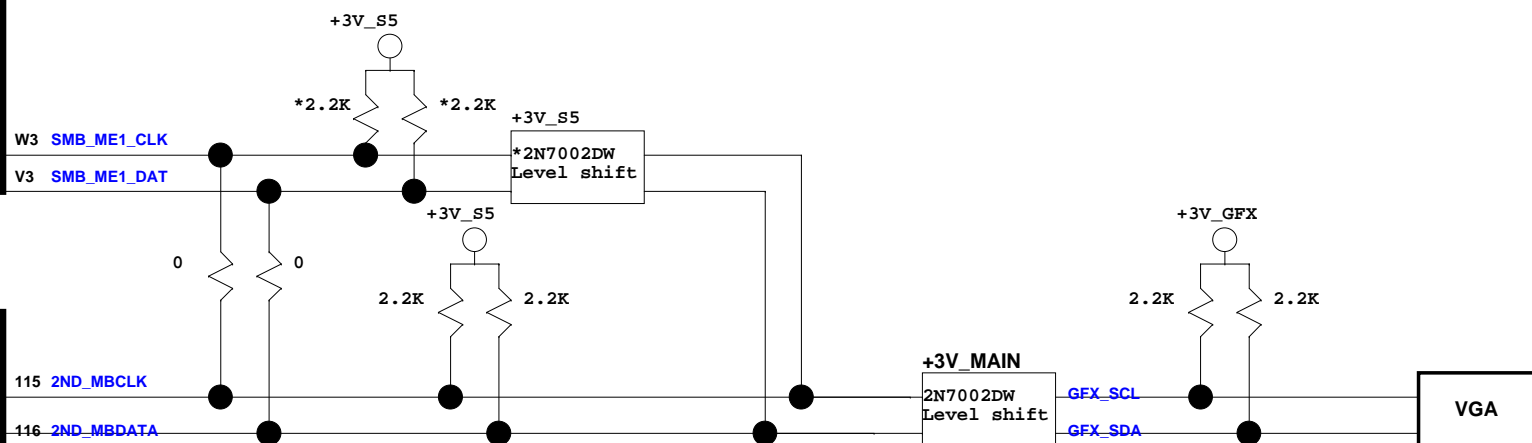
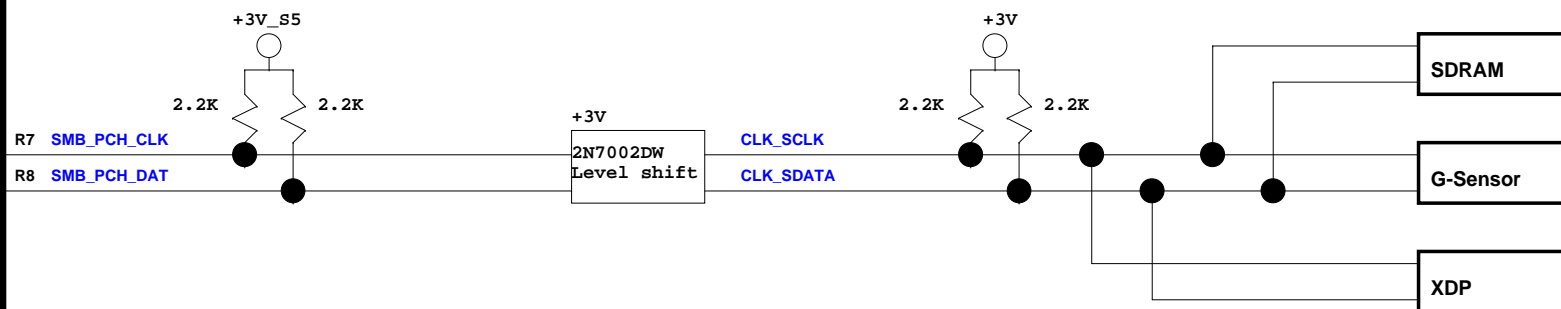








Skylake U

EC  
IT8987CX115 2ND\_MBCLK  
116 2ND\_MBDATA110 MBCLK  
111 MBDATA

CHARGER